A High-Speed Source Follower Type Analog Buffer Circuit Using LTPS TFTs for 2.2-inch qVGA TFT-LCD panel

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Abstract

*A high speed analog buffer using polycrystalline silicon (poly-Si) thin film transistors (TFT) is proposed for 2.2-inch quarter video graphic adapter (qVGA) TFT-LCD panel. Simulation results show that the settling time of the proposed circuit is 10μsec in 2.2-inch qVGA and the power consumption of proposed analog buffer is 25*μW

1. Introduction

Low Temperature Polycrystalline Silicon (LTPS) technology has a potential to integrate the driver circuits of TFT-based displays such as LCD with pixel array on a substrate because it has a higher mobility than amorphous silicon. But the LTPS TFT has some inferior electrical characteristics to single crystal Si transistor, which include low mobility, high threshold voltage and non-uniformity of the electrical properties**.**

To solve those problems, the buffers using low temperature polycrystalline silicon technology can be largely divided into differential type[1], comparator type[2], and source-follower type[3] buffers. Differential type buffers have the problems of input stage mismatching due to the non-uniform electrical characteristics of poly-Si TFTs and comparator type buffers consume large amount of power because of large amount of static current during comparator operation. Because of these reasons source follower type buffers are generally used in most of the data driver in LTPS thin film transistor liquid crystal display (TFT-LCD) for mobile applications[4]. However, conventional source-follower buffers have the problem of slow operation because of decreasing of gate-to-source voltage as the output voltage increases. To overcome this problem, Figure 1 shows a schematic of double compensation buffer

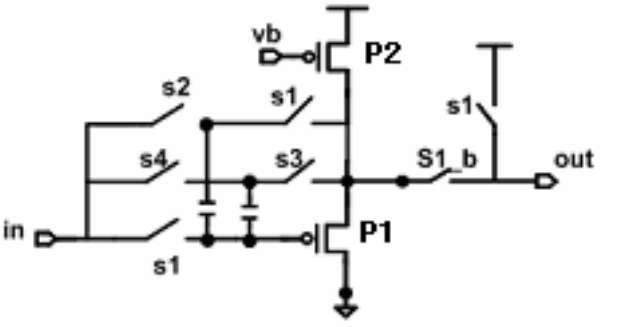


Figure 1. Schematic diagram of output error double compensation analog buffer

a modified source-follower type buffer with double compensation technique has been reported[5], but it still cannot solve the slow operation problem perfectly because it just compensates output error twice with the same concept. Therefore, this paper proposes a new source-follower type buffer with pre-compensation for high speed operation.

2. Proposed circuit

Figure 2 shows a schematic diagram of the proposed buffer. It consists of diode connected n-type TFT, two p-type TFTs and two capacitors. The proposed buffer operates in three phases.

In T0 phase, S1_b switch turns on and the output load is charged to VDD and node A is initially discharged to GND.

In T1 phase, S1_b switches turn off, and S1 switch turns on. S2 switches turn on and input voltage, V_{input}, is applied to node in, where the voltage of node A becomes $V_{input}-V_{thn}$ because of diode connected NTFT. The output voltage is discharged to $V_{input}-|V_{thn}+V_{thp}|$ and the voltage of node B is charged to this voltage. The amount of $|V_{thn}+V_{thp}|$ is very small because the polarity of

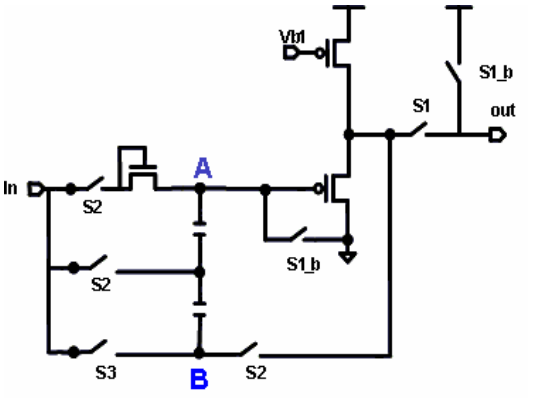
V_{thn} and V_{thp} are opposite, so the diode connected n-type TFT acts as pre-compensation TFT.

In the last T3 phase, S3 switch turns on, so the voltage of node B changes from $V_{input}-|V_{thp}+V_{thn}|$ to V_{input} and the voltage of node A changes from $V_{input}-|V_{thn}|$ to $V_{input}-|V_{thp}|$, so the output voltage is V_{input}.

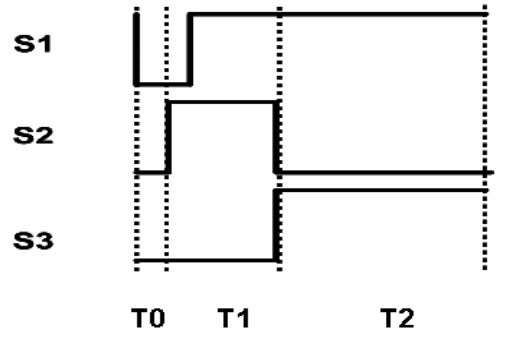
3. Simulation results

We simulated the proposed buffer using LTPS process under the conditions in Table 1.

Fugure3 shows the waveforms of the proposed analog buffer. Output voltage is totally settled in 10μsec. Figure 4 shows the settling time of the double compensation scheme [5] and the proposed scheme, respectively. When the settling time is assumed that the output voltage is reached as 90% of the target voltage, the settling time of the double compensation scheme is 17μsec, while the settling time of the proposed scheme is 10μsec. Therefore, the proposed analog buffer increases the period that DAC drives output directly so that low power operation of the analog buffer can be achieved. If settling time of the analog buffer is reduced, connecting time of DAC is increased. Therefore, the value of the resistors of R-string can be made to be large so that the static current of DAC can be reduced. Figure 5 shows the error voltage of the proposed buffer. The error voltages are less than 0.8 LSB under the condition of 20% variations of threshold voltage and mobility and total power consumption of the proposed analog buffer and DAC is 5.59mW, and it is 82% of that of the double compensation scheme.



(a)



(b)

Figure 2. Schematic and timing diagram of the proposed analog buffer, (a) schematic diagram and (b) timing diagram.

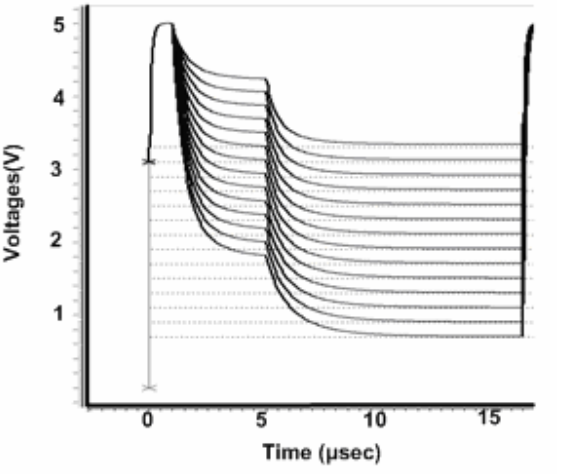


Figure 3. Output voltage waveforms of the proposed analog buffer.

4. Measured results

We fabricated the proposed buffer using a LTPS process and measured its electrical properties under the conditions as shown in Table 2, where the load conditions are determined to suppose a case that the proposed buffer drives a 2.2-inch qVGA(240×RGB ×320) TFT-LCD panel. Figure 6 shows the measured output wave forms of proposed buffer. The settling time of output

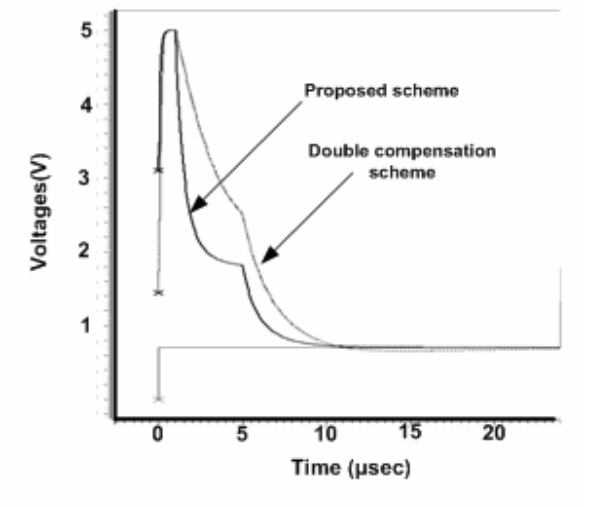


Figure 4. Output voltage waveforms of the proposed and the double compensation schemes.

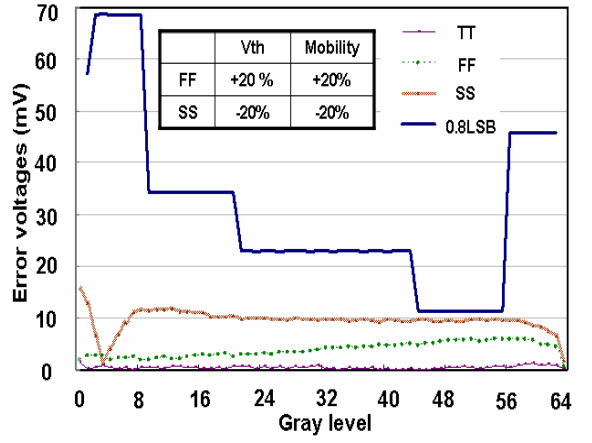


Figure 5. Error voltages of the proposed buffer.

Table 1. Simulation conditions of the proposed buffer

Power supply voltage	10V
Input signal range	1 V~4V
Line time	52μsec
Load condition	C: 12pF and R:900Ω
Threshold voltage	NTFT:1V PTFT:-1.65V
Panel size	2.2-inch
Resolution	qVGA

Table 2. Measured conditions of the proposed buffer

Power supply voltage	5V
Input signal range	0.7V~3.3V
Line time	52μsec
Load condition	C: 12pF and R:900Ω
Panel size	2.2-inch
Resolution	qVGA

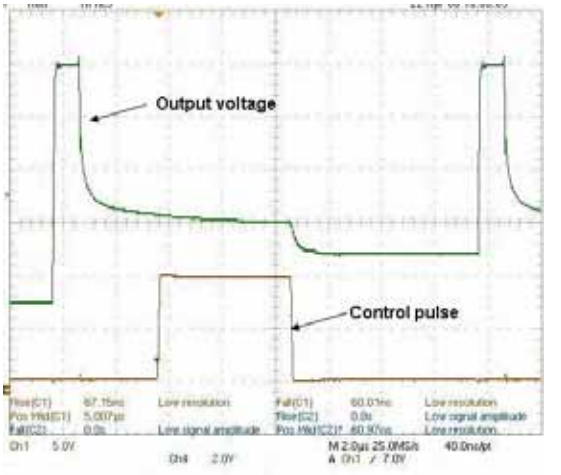


Figure 6. Measured waveforms of the proposed buffer.

voltage is reached to 10 μsec. The measured output waveforms of the analog buffer is shown where the line time is 16μsec and the load capacitance is 12pF. Therefore, the implemented analogue buffer can be applied to 1:3 de-multiplexing and since there is sufficient margin in the driving time, the buffer can also be used for a larger panel and high resolution.

5. Conclusions

High speed source follower type analog buffer circuit is proposed. Measured and simulated results show that the driving speed does not become slow even when an output voltage approaches a target voltage and the output voltage is perfectly settled. The settling time of the proposed analog buffer is 10μsec, which is 60% of that of the previous double compensation one. By using this buffer, it is expected that a low power

and high quality display can be realized in LTPS technique

6. Acknowledgements

This research was supported by a grant (F0004111) from the Information Display R&D Center, one of the 21st Century Frontier R&D Program funded by the Ministry of Commerce, Industry and Energy of the Korean Government.

7. References

[1] M. Ker, C. Deng, and J. Huang, “On panel Design Technique of Threshold Voltage Compensation for Output Buffer in LTPS Technology,” in *SID Int. Sym. Digest of Tech. papers*, 2005.

[2] Y. S. Yoo, J. Y. Choi, H. S. Shim, and O. K. Kwon, “A high Accurate Analog Buffer Circuit using Low Temperature Poly-Si TFT” in *SID Int. Sym. Digest of Tech. papers*, 2004 .

[3] J. Jeon, O. K. Kwon, "A New Digital Driving Scheme for Poly-Si TFT-LCD Panels," in *SID Int. Sym. Digest of Tech. papers*, 1999.

[4] N. Toyozawa, Y. Nakjima, H. Yoshine, S. Noichi, K. Yuda, S. Toriyama, A. Ogawa, T. Yoshikawa, and Y. Maki, “Low Power Integrate Circuit Technologies Using Low Temperature Poly-Si TFTs for Mobile Device Application," in *SID Int. Sym. Digest of Tech. papers*, pp.686-689, 2002.

[5] Y. Kida, Y. Nakajima, M. Takatoku, M. Minegishi, S. Nakamura, Y. Maki, T. Maekawa, "A 3.8 inch Half-VGA Transflective Color TFT-LCD with Completely Integrated 6-bit RGB Parallel Interface Drivers," in *Eurodisplay Int. Symp. Digest of Tech. papers*, pp.830-834, 2002.