An Ultra Low-Power and High-Speed Down-Conversion Level Shifter Using Low Temperature Poly-Si TFTs for Mobile Applications

Soon-Sung Ahn, Jung-Hwan Choi, Byong-Deok Choi, and Oh-Kyong Kwon
Division of Electrical and Computer Engineering, Hanyang University
17 Haengdang-Dong, Seongdong-Gu, Seoul, 133-791, Korea
Phone: +82-2-2220-0359, E-mail: okwon7@chol.com

Abstract

An ultra low-power down-conversion level shifter using low temperature poly-crystalline silicon thin film transistors is proposed for mobile applications. The simulation result shows that the power consumption of the proposed circuits is only 17% and the propagation delay is 48% of those of the conventional cross-coupled level shifter without additional area. And the measured power consumption is only 21% of that of the cross-coupled level shifter.

1. Introduction

System on a Panel (SoP) using low temperature poly-crystalline silicon (LTPS) thin film transistors (TFTs) has an advantage of low cost by integrating peripheral circuits on the panel. However, the power consumption of poly-Si integrated circuits on a panel tends to be higher than that of single-crystalline silicon ICs because of higher supply voltage due to high threshold voltage and low mobility of poly-Si TFTs[1]. Especially, cross-coupled level shifter (CCLS) shown in Figure 1(a) consumes enormous power because the large amount of short-circuit current flows during transition time[2]. The power consumption of an unit level shifter block is very important because every column requires N level shifters in N-bit gray level display, and the power of level shifter array is about 10 to 15% of the total power consumption of a data driver in 2.2-inch qVGA OLED panel. This is why there have been many efforts to reduce power consumption of level shifters. Although the level shifter by bootstrapping technique[3] shown in Figure 1(b) remarkably reduces power consumption by capacitor-coupling structure, but its layout area increases by additional two capacitors.

To overcome aforementioned problems, this paper proposes an ultra low-power and high-speed level shifter in 2.2-inch qVGA OLED panels.

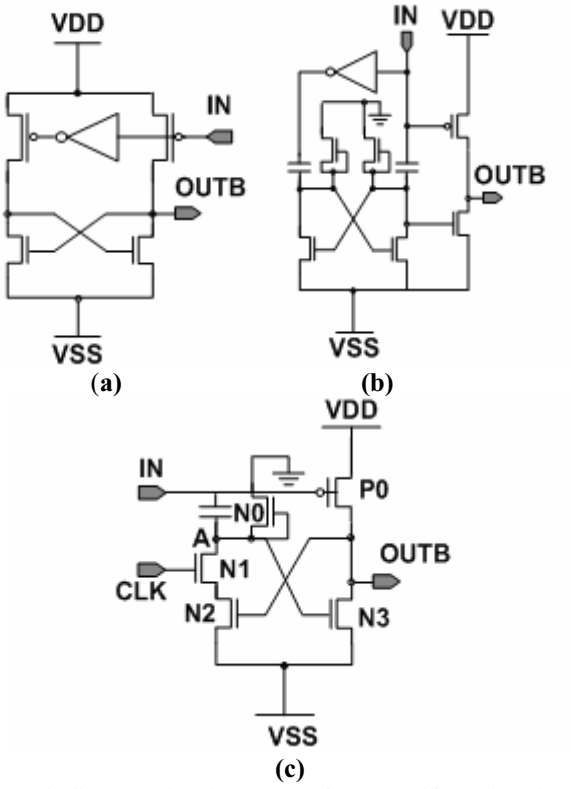


Figure 1. Schematic diagrams of level shifter circuits (a)cross-coupled level shifter(CCLS), (b)level shifter by bootstrapping technique, (c)proposed level shifter.

2. Operation

The schematic diagram of the proposed level shifter circuits is shown in Figure 1(c), and its waveforms are shown in Figure 2. The circuit converts the input, IN, which swings from GND to VDD to the output, OUTB, which swings from VDD to VSS, where the voltage levels of the VDD, GND, and VSS are described in Figure 2.

If the IN is LOW and the CLK is HIGH, P0, N1 and N2 turn on, so the node A becomes VSS. Now the input rises to HIGH during LOW period

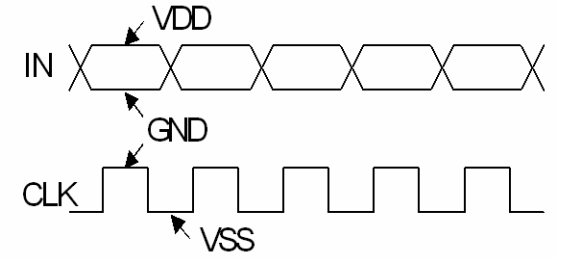


Figure 2. Input signals and their voltage levels of proposed level shifter.

of the CLK. Because node A simultaneously rises to GND by capacitor-coupling, P0 turns off and N3 turns on almost immediately. While OUTB is VSS, node A is separated from VSS even if CLK turns N1 to be on. In case that the input falls to LOW, node A becomes VSS. Consequently P0 turns on and N3 turns off. And while the CLK is HIGH, the node A is reset by VSS. Diode connected N0 makes voltage of node A less than (GND + Vth).

3. Simulation results

Figure 3 shows that the propagation delay of the proposed level shifter is shorter than that of CCLS. The proposed one has about 7ns of propagation delay, which is reduced to 47.8% compared to CCLS. Moreover, from Figure 4, the proposed one is more stable in corner conditions.

The power consumption of the proposed one is just 16.91% of that of CCLS. If we consider the power to generate the CLK signal which is made by a common CCLS and an inverter for buffering 12pF load of a long line, whose outputs swing from VSS to VDD and from VSS to GND, respectively, its power consumption is 18.13% of that of CCLS. The proposed level shifter has lower peak current than CCLS as shown in Figure 5. Table 1 summarized simulation results of the power consumptions and propagation delays according to the level shifter circuit types.

Although the proposed level shifter has additional capacitor, its layout area is almost same as that of CCLS because the number of interconnection lines is reduced to half of that of CCLS and all the TFTs of the proposed level shifter can be designed as minimum-size. Figure 6 shows each layout diagrams of the two level shifter circuits, CCLS and the proposed type.

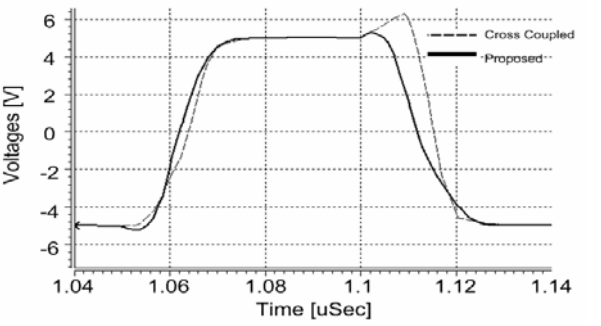


Figure 3. Simulated waveforms of output voltages in normal condition (Input frequency is 10Mhz to show rising and falling in a window).

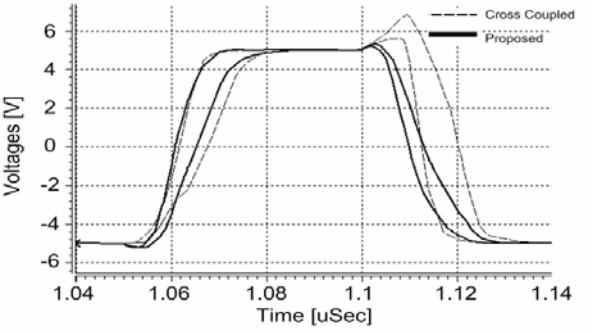


Figure 4. Simulated waveforms of output voltages in corner conditions (Input frequency is 10Mhz to show rising and falling in a window).

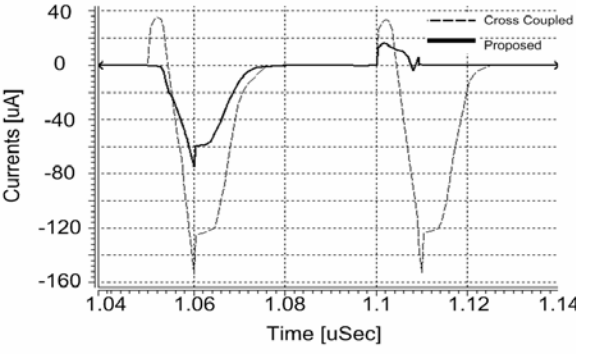
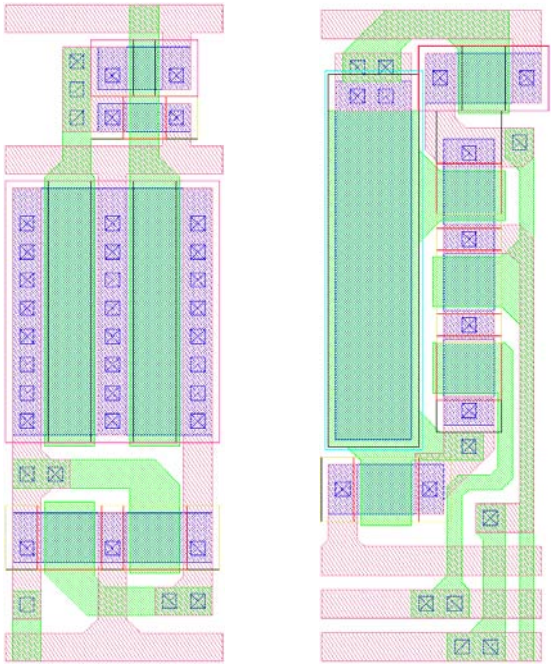


Figure 5. Simulated waveforms of currents in VDD (Input frequency is 10Mhz to show rising and falling in a window).

Table 1. Comparison of power consumptions (per a level shifter in 62.5kHz input frequency) and propagation delays from simulation result.

	Power consumption	Propagation delay	
		Rising	Falling
Figure 1(a)	1.153uW	14.51ns	15.11ns
Figure 1(b)	0.190uW	11.72ns	13.08ns
Proposed	0.195uW	7.045ns	7.115ns



(a) (b)

Figure 6. Layout diagrams of level shifter circuits. (a) cross-coupled level shifter. (b) proposed level shifter.

4. Measured results

The proposed level shifter were implemented in 2-μm LTPS TFT process. Figure 7 shows measured waveforms of proposed level shifter when VDDH supply voltage is 5V. The power consumption of level shifters were measured according to various supply voltage and frequency conditions and the summarized result shown as figure 8. The power consumption of the proposed one is 21.4% of that of CCLS when supply voltage is 5V. Increasing VDDH and IN whose swing range still remain 5V, the proposed level shifter consume less power at higher supply voltage. So the power consumption of the proposed one is 16.7% of that of CCLS when supply voltage is 10V.

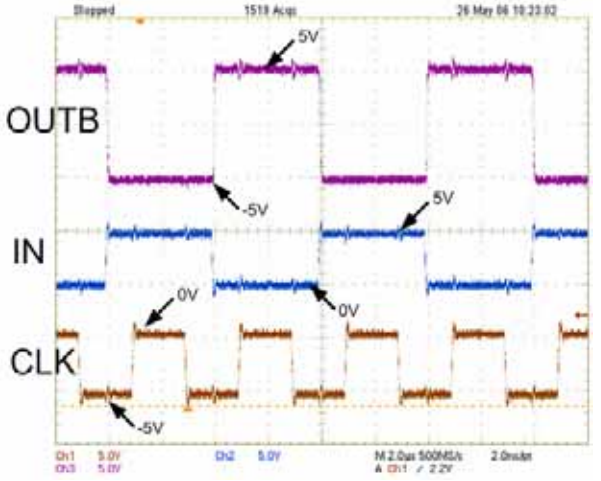


Figure 7. Measured waveforms of proposed level shifter at VDDH supply voltage of 5V.

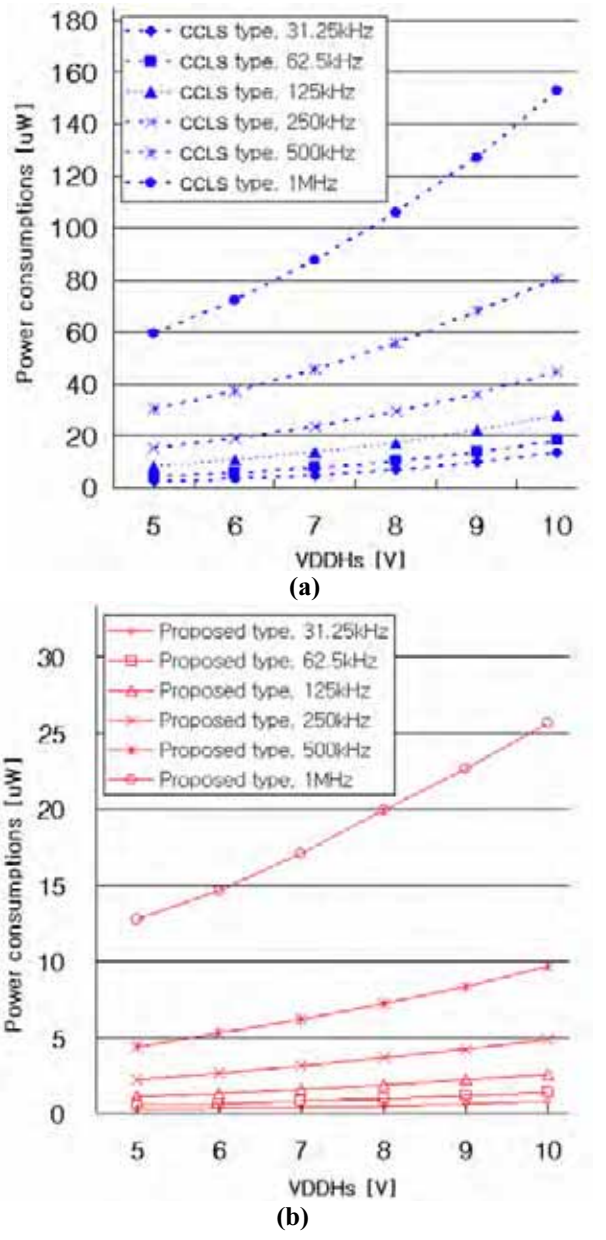


Figure 8. Measured results of power consumption. (a) power consumption of cross-coupled level shifter varying supply voltage and frequency. (b) power consumption of proposed level shifter varying supply voltage and frequency.

5. Conclusions

A typical cross-coupled level shifter brings about the quite large short-circuit current and the long propagation delay. So, we have proposed area-efficient capacitive-coupled level shifter, and it dramatically reduces the short-circuit current and the propagation delay with stable operation. The power consumption of the proposed level shifter is only about 1/6, and the propagation delay is about 1/2 of those of the cross coupled level shifter without area increase compared with the conventional cross-coupled level shifter. And the measured power consumption is only about 1/5 of that of the cross-coupled level shifter.

Table 2. System specification.

Resolution	2.2” qVGA
Color depth	6bit RGB
DAC type	De-coder type with de-multiplexing
# of level shifter	240 x 6
Level shifter input	0 ~ 5V
Level shifter output	-5 ~ 5V
Load condition	Minimum size inverter

6. Acknowledgements

This research was supported by a grant (F0004111) from the Information Display R&D Center, one of the 21st Century Frontier R&D Program funded by the Ministry of Commerce, Industry and Energy of the Korean Government.

7. References

[1] H. Haga, H. Tsuchi, K. Abe, N. Ikeda, H. Asada, H. Hayama, K. Shiota, N. Takada, "A Parallel Digital-Data-Driver Architecture for Low-Power Poly-Si TFT-LCDs," in *SID Int. Symp. Digest of Technical Papers*, 2002, pp. 690-693.

[2] F. Ishihara, F. Sheikh, B. Nikolic., “Level Conversion for Dual-Supply Systems,” *IEEE Tran. On VLSI Systems,* vol. 12, no. 2, Feb. 2004, pp. 185-195.

[3] S. C. Tan, X.W. Sun, "Low power CMOS level shifters by bootstrapping technique," *Electronics Letters,* vol. 38, no.16, pp. 876-878, August, 2002.

[4] A. Bellaouar, M.I. Elmasry, *Low-Power Digital VLSI Design,* Kluwer Academic Publishers, 1995.