Amorphous Silicon Gate Driver with High Stability

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Abstract

Integrated a-Si:H gate driver with high reliability has been designed and simulated. The proposed a-S:H gate driver has only one reset transistor under AC driving for P and output node. These reset transistors show much less degradation than those under DC driving. The simulation results show that the lifetime and response time are improved significantly compared with those of the prior circuit.

1. Introduction

Integrating of driver circuits in TFT backplane is of increasing interest because of many advantages such as overall cost reduction, compactness and mechanical reliability [1-4]. Since the mobility of the poly-Si TFT is high enough for driver integration, it can be used in system on glass (SOG), where the memory, sensor, microprocessor and control circuits can be integrated in addition to drivers. However, the manufacturing cost of poly-Si TFT backplane is much higher than that of a-Si:H one.

On the other hand, the integrated circuit using a-Si:H TFT has several advantages. First, most of the TFT-LCD manufacturers are based on a-Si:H TFT technology. Second, a-Si:H TFT process is suitable for large area applications because of its low cost, low temperature processing and better uniformity over large area substrates. Third, the module cost can be reduced by eliminating the driver IC's and related process.

However, there are two important properties designing integrated circuit using a-Si:H TFT. One is the low mobility and high threshold voltage. The other is the instability of a-Si:H TFT which is more critical issue. Threshold voltage of a-Si:H TFT increases with increasing both operation time and gate voltage.

In this work, we propose a new a-Si:H gate driver with less threshold voltage (V_{th}) shift,

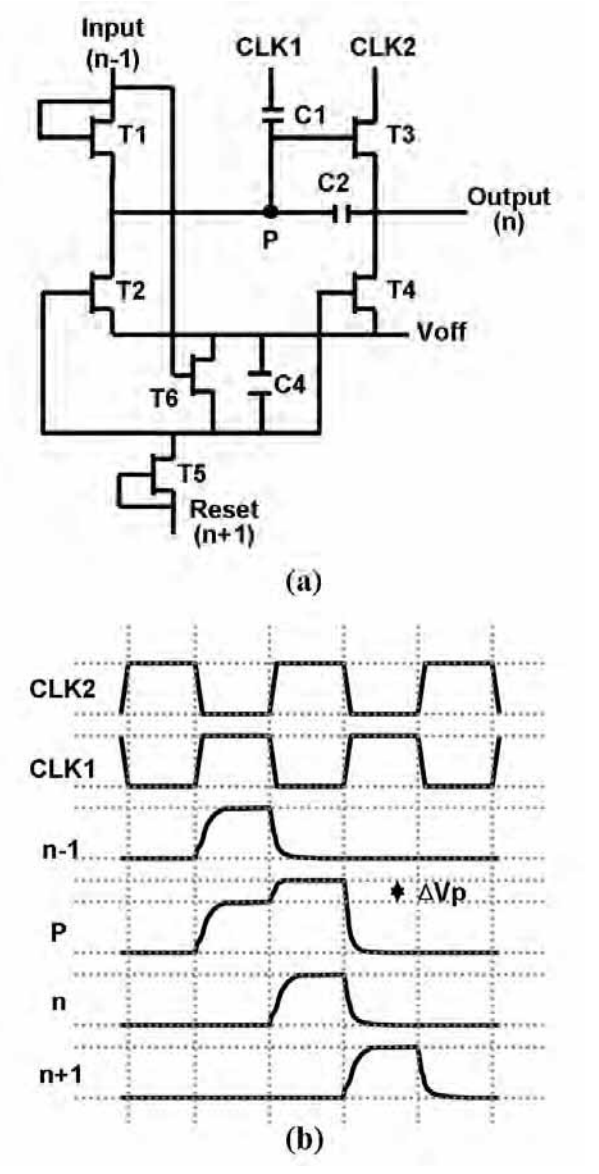

Figure 1. Schematic diagram of a prior gate driver unit developed by our group : (a) the prior a-Si gate driver with DC Bias and (b) timing diagram of gate driver.

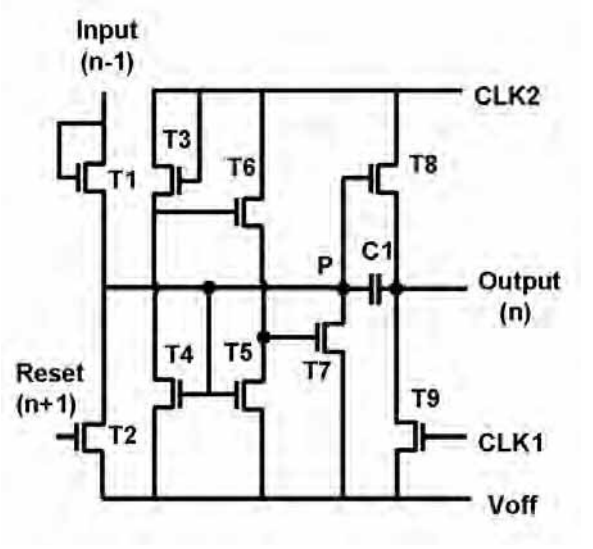

Figure 2. Schematic diagram of the proposed a-Si:H gate driver.

longer life time and more simplified structure, and simulate the operational lifetime by Spice simulation tool.

2. Results and Discussion

Figure 1 shows the prior gate driver with DC biased reset transistors and its timing diagram developed by our group [5]. Its advantage is to prevent output and P node from floating by reset transistors under DC bias. However, it has two problems. One is the Vth shift of reset transistor (T2, T4), because the gates of reset transistors are under DC bias. The other is the coupling capacitor (C1) which is to eliminate the positive fluctuation of the P-node occurred by capacitive coupling with CLK2. However, the coupling capacitor (C1) suppresses boosting voltage of P node and increases the rising and falling times of the output potential. Therefore, we propose a new gate driver circuit to overcome these problems.

Figure 2 shows the schematic diagram of the proposed circuit. It is composed of nine TFTs and one capacitor. The reset transistors (T7, T9) are under AC driving, which results in much less threshold voltage shift compared to those under DC driving. Reset transistors T7 and T9 are turned on alternatively to discharge P and output node potentials.

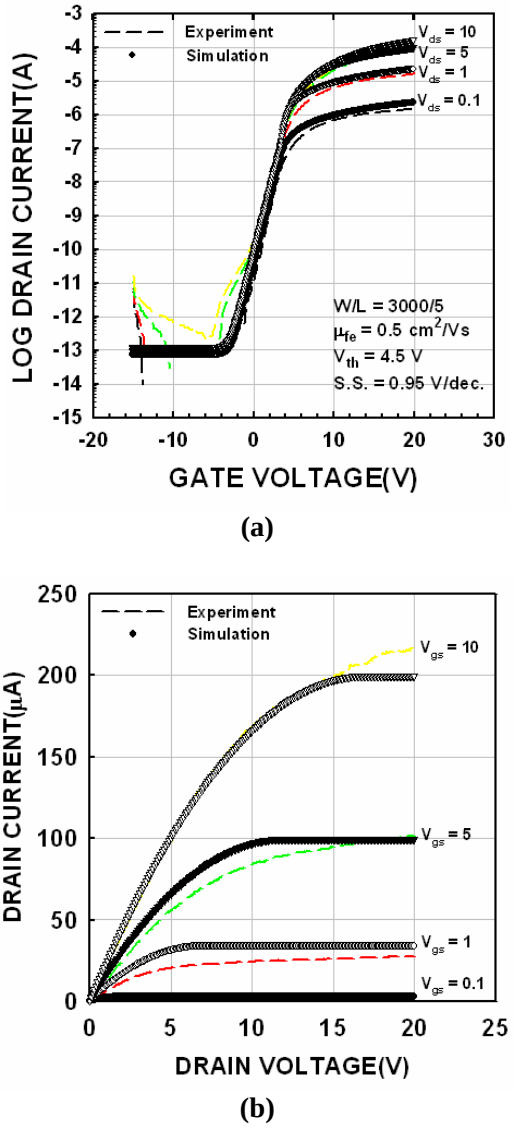

Figure 3. The measurement & simulation results of a-Si:H TFT which is manufactured by our group : (a) the transfer characteristics and (b) output characteristics

The operation of the proposed gate driver circuit is as follows. When input signal is high, P node is charged by input signal and then as CLK2 is changed from low to high, P node voltage is boosted up, due to gate-drain capacitive coupling of T8. Therefore, the output driving ability is achieved by bootstrapping voltage of the P node. At this time, the high voltage of P node is applied to the gates of T4 & T5 simultaneously.

Table 1. Model parameters of a-Si:H TFT used for a-Si:H gate driver.

Name	Symbol	Value	Unit
Channel width	W	3000E-6	m
Channel length	L	5E-6	m
Thin oxide thickness	TOX	300E-9	m
Drain-source shunt resistance	RDS	1E29	Ω
Surface mobility	U0	0.5	cm²/Vs
Zero-bias threshold voltage	VTO	4.5	V
Bulk junction saturation current	IS	0	A
State density of the surface	NFS	1.3E12	cm⁻²

Therefore, T7 is turned off and high voltage is kept up at the P node. After generating output voltage, P node voltage is discharged when the reset signal (n+1) is applied to the gate of T2 and then T4 & T5 are turned off. Since then, the P node is alternately discharged through T7 by CLK2 signal. When CLK2 is high, P node is discharged at the low level voltage. When CLK2 is changed from high to low, P node is floated, and then, P node voltage has negative fluctuation caused by capacitive coupling of T8. When CLK1 is changed from high to low, output has the same negative fluctuation by capacitive coupling of T9. There is no positive fluctuation which is the critical issue of the conventional circuit. The negative fluctuation (Circle C, in Fig. 3) does not have influence on output voltage characteristics.

Figure 3 shows the modeling results of a-Si:H TFT which is manufactured by our group. Table 1 shows the modeling parameters of an a-Si:H TFT used for gate driver [6]. We simulated the output voltages of the a-Si:H gate driver with these model parameters. We used a MOSFET model for the a-Si:H TFT with appropriate parameters in a PSPICE simulation tool.

Figure 4 shows the simulation results of output voltage of the prior and proposed circuits, according to aging time. The lifetime of the proposed circuit is much longer than that of the prior circuit. In Fig. 4, the circle A is caused by the coupling capacitor (C1). The circle B is caused by the degradation of pull-down transistors. (T2, T4 in Fig. 1) The reset transistors under AC driving result in much less threshold voltage shift and thus longer lifetime.

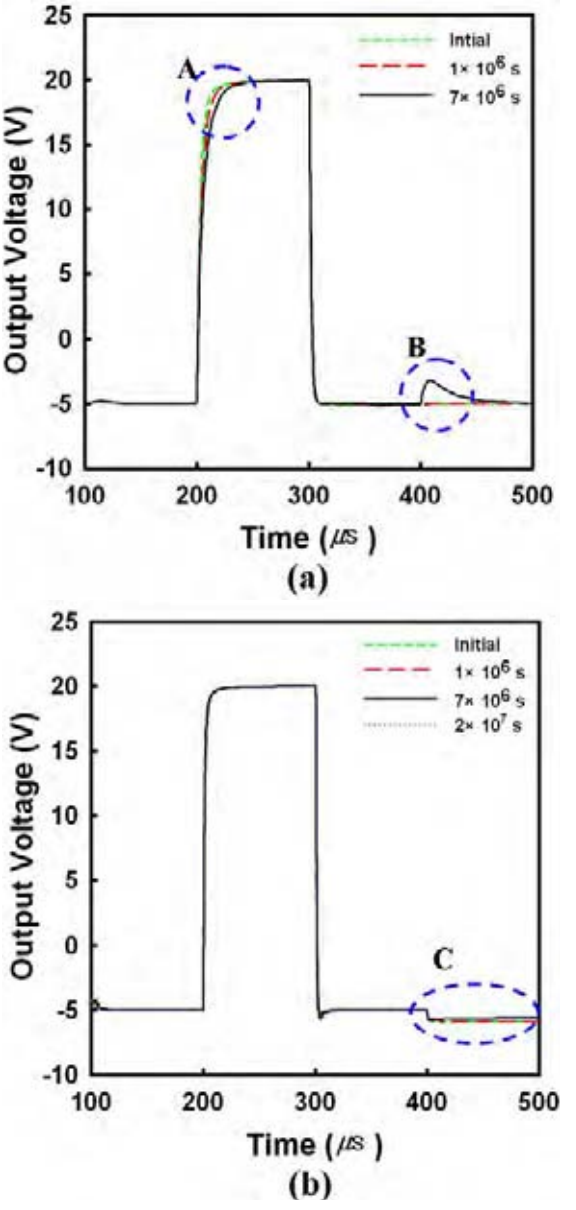

Figure 4. The simulation Results of output voltage according to aging time: (a) The output waveform of the prior gate driver unit; (b) The output waveform of the proposed gate driver unit.

Figure 5 shows the rising and falling times of the output voltage, which is improved significantly in the proposed circuit. The fast response time is achieved by eliminating coupling capacitor (C1) which suppresses the boosting voltage of P node.

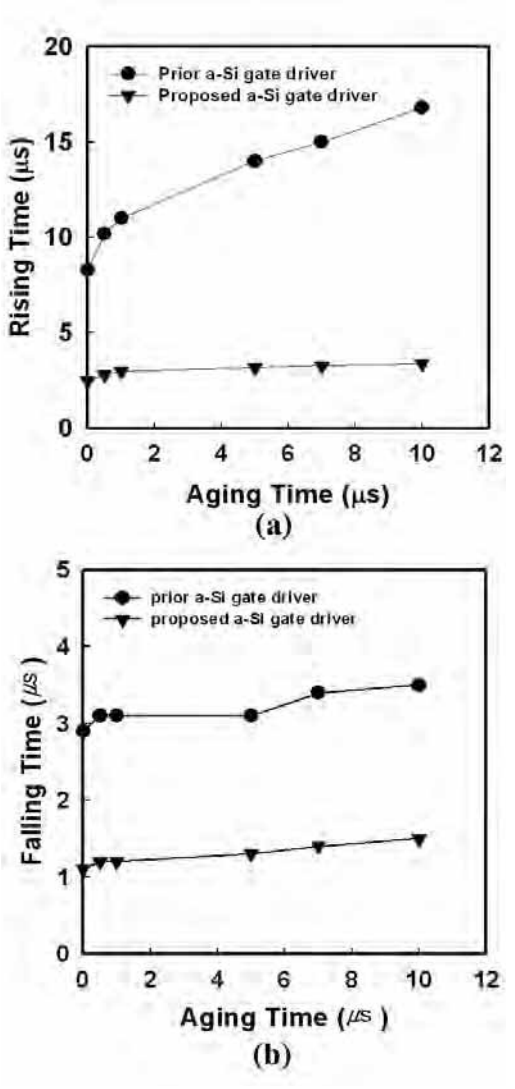

Figure 5. Simulation results according to aging time. (a) Output voltage rising time variation between the prior and proposed circuit. (b) Falling time variation between the prior and proposed circuits.

3. Conclusion

In this work, we proposed a new a-Si:H gate driver with less threshold voltage (Vth) shift, longer life time and more simplified structure. As shown in simulation results, the lifetime and response time are improved remarkably in the proposed circuit. In addition, Most of the a-Si:H gate driver units have two reset transistors under AC driving at the output and P nodes respectively [7-9]. However, in our circuit, only one reset transistor is used for charging and discharging at the output and P nodes. The pull-down TFTs turn on alternately for maintaining a gate line and P node at low voltage. As a result, the area of the integrated circuits and the number of TFTs are reduced without degrading the stability.

4. References

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