Source-Follower Type Analog Buffer Using Low Temperature Poly-Si TFTs for AMLCDs

• ***Bo-Ting Chen[a]*, Ya-Hsiang Tai[b], Ying-Jyun Wei[a], Chun-Chien Tsai[a], Hsu-Hsin Chen[a], Chun-Yao Huang[c], Yu-Ju Kuo[d], and Huang-Chung Cheng[a]***

[a] Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan

[b] Department of Photonics and Display Institute, National Chiao Tung University, Hsinchu 300, Taiwan

[c] Panel Design Dept., R&D Design Division, Central Research Institute, Chunghwa Picture Tubes, LTD.

[d] LCD Product Technology Div., Array Cell Design Department, AU Optronics Corporation, Hsinchu 300, Taiwan

(*corresponding author: Bo-Ting Chen, Phone: +886-3-5712121-54218, Email: toni.ee87@nctu.edu.tw)

Abstract

A new source follower circuit for the integrated circuit of AMLCDs is proposed. Active load is added and calibration operation is applied to compensate the circuits. Proposed circuit is capable of minimizing the variation from both timing and device variations through measured results, the uniformity and bias effect are discussed.

1. Objectives and Background

Low-temperature poly-Si thin-film transistors (LTPS TFTs) have attracted much attention for integrating driver circuits of TFT-based flat panel displays such as AMLCD and AMOLED [1]-[7]. In a poly-Si TFT-LCD, poly-Si TFT is used to implement not only the driving circuits but also the pixel array on a single glass substrate. Such integration allows us to reduce system cost and realize compact, highly reliable displays.

Among the many driving circuits employing LTPS TFTs, the output buffer is indispensable to drive the large load capacitance of the data bus. There are several requirements for the output buffer for a flat panel display column driver [1]. Since thousands of output buffers are necessary for a poly-Si TFT-LCD, it is very important to develop special analog buffers dealing with the device non-uniformity. Variations of LTPS-TFTs will cause the real output voltage not the target value and lead to the wrong gray scale. Thus, the output deviation must be decreased as possible. Among many types of output buffer circuit for displays, source follower is considered an excellent candidate for the output buffer circuit for the "System on Panel" application since its simplicity and low power dissipation. [2] – [7].

2. Results

Figure 1(a) shows the threshold voltage variation of thirty poly-Si transistors fabricated in a factory and Figure 1(b) shows the field-effect mobility variation. It is observed that the LTPS TFTs have 1 V threshold voltage maximum difference and 36 $cm^2/v{\cdot}s$ field-effect mobility maximum differences.

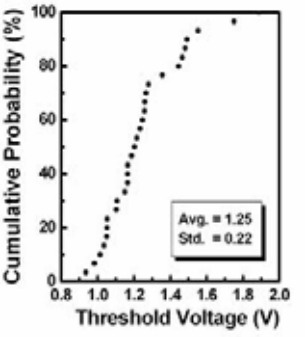

Fig. 1(a)

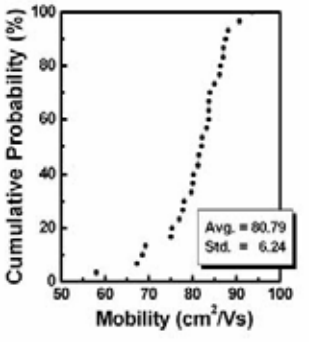

Fig. 1(b)

Fig. 1. Thirty poly-Si transistors of (a) threshold voltage variation; (b) field-effect mobility variation

The typical model of the LTPS TFTs used in this work is represented by the RPI parameters. In this work, the data line capacitance loading is assumed to be 20pF corresponding to a 2-inch QVGA LCD. A conventional source follower and its output waveform are shown in Figure 2. It is observed that the final output voltage is not

kept constant, but exceeds the value of Vgs-Vth expected in principle. It is attributed to the sub-threshold current of the LTPS TFT. Consequently, it will be sensitive to the charging time applied for various product specifications. An active load is studied and added to eliminate this phenomenon. It is distinct that unsaturated phenomenon of the output voltage is suppressed successfully in Figure 3. The offset voltage difference of conventional source follower is larger than source follower with active load with different charging time. Although offset voltage of source follower with active load larger than conventional source follower, it can be eliminated by gamma correction [4]. Therefore, the charging time variation-tolerant characteristic of source follower with active load is superior to the conventional source follower.

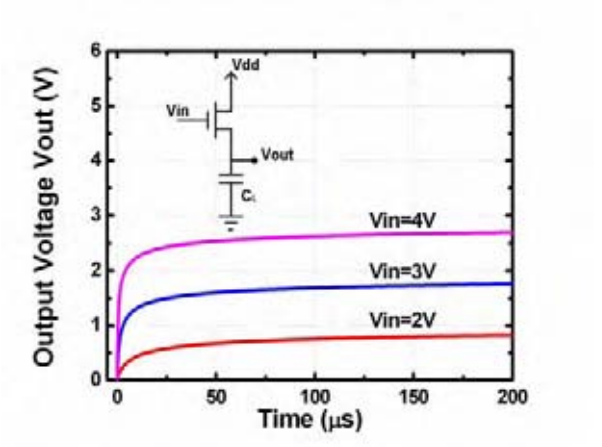

Fig. 2. Conventional source follower and its output waveform simulation results

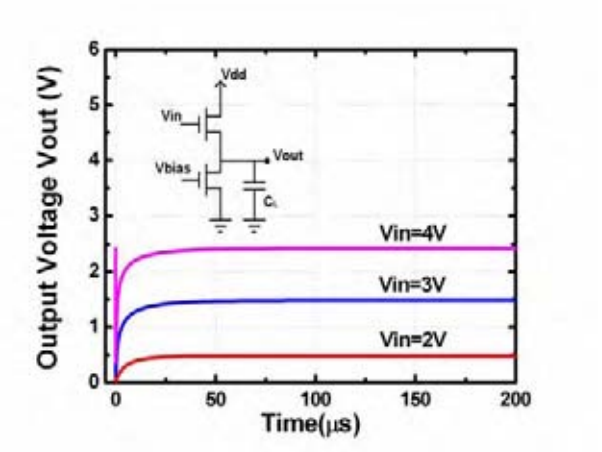

Fig. 3. Schematic of conventional source follower with an active load and its output waveform simulation results

It is obvious that the buffer circuit suffers from huge variations and output voltage is not Vin-Vth due to the electrical variations of LTPS TFT mentioned in Figure 1. Therefore, we proposed a new analog buffer in this article for the compensation of the device variation [6] [7]. Figure 4 shows a schematic of the proposed analog buffer consisting of two transistors, a capacitor, and four switches. The gate voltage of the TFT as the active load is biased at Vbias. The driving schemes are as follows. During first operating period, S1 and S2 are turned on, and S3 and S4 are turned off. There by, a voltage corresponding to the threshold voltage of driving TFT, the threshold voltage of the active load and the bias voltage is stored in Cvt. After sampling period, S3 and S4 are turned on and S1 and S2 are turned off, then the voltage at the gate of the driving TFT is held. Thus, the output voltage is compensated by the voltage stored in Cvt previously. The output voltage variation also decreases drastically.

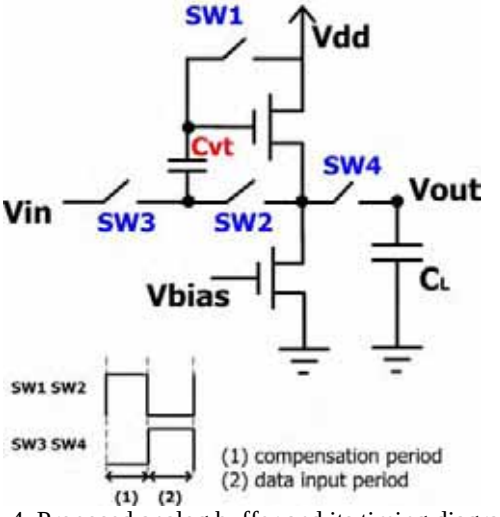

Fig. 4. Proposed analog buffer and its timing diagram

Figure 5 shows the Monte Carlo simulation output waveform of the proposed analog buffer when input voltage is 2V, 3V, and 4V. It is clear that the output variation is comparatively small regardless of the large variation of LTPS-TFTs characteristics.

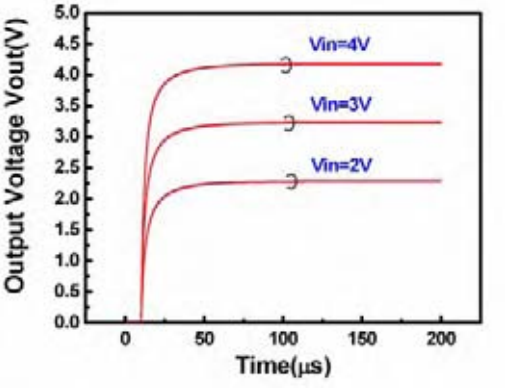

Fig. 5. Monte Carlo Simulation output waveform of the proposed analog buffer when input voltage is 2V, 3V, and 4V.

The proposed analog buffer is fabricated using a LTPS CMOS process and measured to study the performance of the analog buffer. The fabrication process is described as follow. A buffer oxide and 500Å-thick a-Si were firstly deposited on the glass substrate sequentially. Then the amorphous silicon thin film was crystallized to poly-crystalline silicon film by KrF excimer laser annealing. After the active region was defined, the channel doping was carried out for adjusting the threshold voltage of n-type TFT. Then, high dose ion implantation was executed to source/drain regions of n-type TFT. Next, 1000 Å-thick gate oxide was deposited by plasma enhanced chemical vapor deposition (PECVD). A 3000Å-thick Cr film was deposited next. Then, the gate oxide and the Cr film were etched to form the gate electrode. Next, a high dose self-aligned ion implantation was executed to form source/drain regions of p-type TFT. Then a 4000Å-thick SiNx was deposited by PECVD as interlayer. Finally, the test circuits for the proposed analog buffer were accomplished after the contact holes formation and the 4000Å-thick Cr metallization.

Figure 6 shows comparison the offset voltage versus input voltage curve of the conventional and proposed analog buffers. Obviously the offset voltage of conventional analog buffer is large compared with proposed analog buffer.

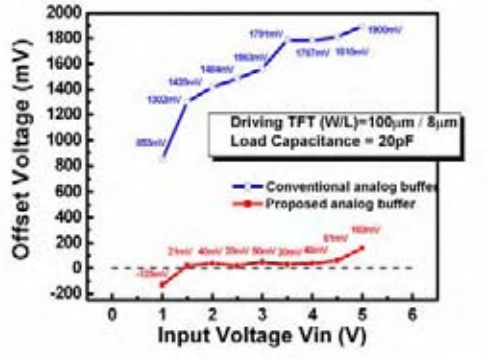

Fig. 6. Comparison the measured offset voltage versus input voltage curve of the conventional and proposed analog buffer

3. Impact

The proposed analog buffer output deviation is controlled under 50 mV mostly regardless of threshold voltage variation which is extremely good results. The Figure 7 shows that offset voltage of conventional analog buffer suffers huge variations and the proposed analog buffer has small output variability and excellent uniformity after non-uniformity calibration.

The Figure 8 shows the comparison of the offset voltage versus bias voltage curve of the simulation and measured results when input voltage 2V. It is observed that the measured result trend is close to the simulation results. The larger bias voltage is the larger offset voltage is. Proper design of the bias voltage is required to achieve total performance.

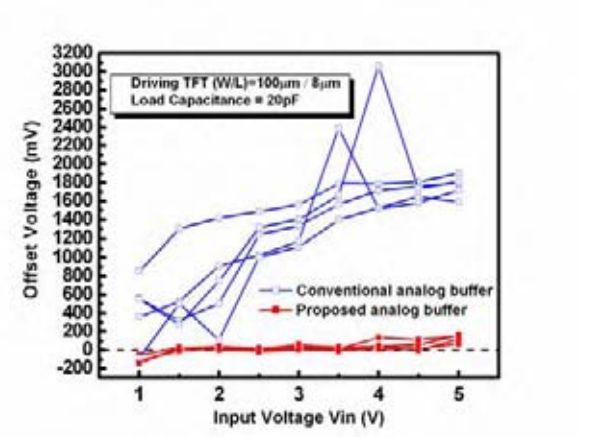

Fig. 7. Offset voltage variation of five sets of analog buffer circuits are compared between the conventional and proposed analog buffer circuits with different input voltages measured results

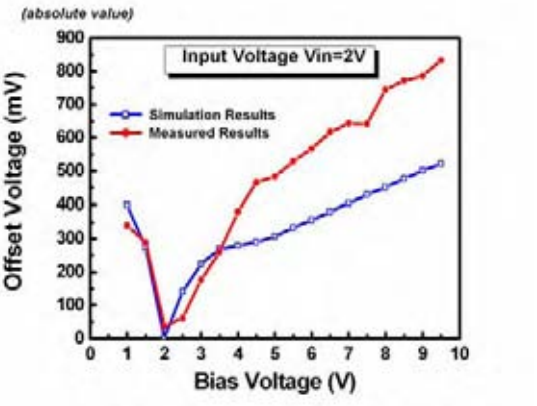

Fig. 8. Comparison of the offset voltage versus bias voltage curve of the simulation and measured results when input voltage 2V

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