Organic thin film transistors with an organic/high-*k* inorganic bilayer gate dielectric layer

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Abstract

Pentacene thin film transistors (OTFTs) on flexible polyimide substrate using electroplated gate electrode and organic/high-k inorganic bilayer gate dielectric layer. Incorporation of thin atomic-layer deposited HfO_2 layer on the PVP organic gate dielectric layer reduced the gate leakage and as a result enhanced the current on/off ratio.

1. Introduction

Organic thin film transistors (OTFTs) on flexible substrate can be applied to low cost sensors, smart cards, and backplane of flexible displays. Electrical performance of flexible OTFTs including current on/off ratio and field-effect channel mobility is critically dependent on the physical properties of gate insulating materials. Gate dielectric layers of organic, inorganic, organic/inorganic bi-layer, and organic/inorganic nano-composite layers can be applied to flexible devices [1,2]. Among those, the organic/high-*k* inorganic bilayer gate dielectric film can possibly provide the advantages including the flexibility by the organic layer as well as the low-leakage current level by ultra-thin high-*k* inorganic layer.

In this work, flexible bottom gated organic thin film transistors were fabricated using pentacene as a semiconducting layer and electroplated nickel (Ni) as a gate electrode on polyimide substrate. Electroplated gate electrode formed on the plasma-treated organic substrate provides a good adhesion [3]. In order to improve electrical characteristics at the device, we employed polymer/high-*k* oxide bilayer structure as a gate dielectric material. First, poly(4-vinyl phenol) (PVP) as an organic gate dielectric layer was deposited by spin coating after Ni gate electrode formation. Formation of Ni gate electrode was electroplated on patterned negative PR on sputtered Cu/Cr seed layer using DC magnetron

sputter. Ultra-thin (≅ 10 nm) HfO_2 as a high-*k* dielectric deposited by ALD (atomic layer deposition) on the spin-coated PVP layer. ALD of HfO_2 layer was carried out at the substrate temperature of 220 ~ 240 °C. Pentacene as a semiconductor layer was thermally evaporated on the gate dielectric layer using a shadow mask in vacuum chamber at the substrate temperature of 80℃ and then the thermal evaporation of gold source and drain electrodes was followed. The OTFT devices with no ALD HfO_2 layer were also fabricated. The channel length varied from 10 to 110 μm, and the channel width was 800 μm. Electrical properties of fabricated OTFT were characterized by I-V measurements.

2. Results

After deposition of the PVP dielectric layer and the HfO_2/PVP bilayer on Si substrate, surface morphology of each layers was measured (not shown here). Surface rms roughnesses of PVP layer and bilayer were 0.3 and 0.27 nm, respectively. Surface morphology of HfO_2/PVP bilayer gate was slightly smoother than that of the gate with only PVP layer.

After deposition of the pentacene on organic and organic/inorganic bilayer gate dielectric on gate electrode, surface morphology of the pentacene layers was measured using AFM. Fig. 1(a) shows surface morphology of the pentacene layer on the PVP organic gate dielectric. Generally, grain size of pentacene was approximately over 1 ㎛. However, surface morphology of the pentacene layer on the HfO_2/PVP bilayer shows smaller grain size compared to pentacene on PVP layer as shown Fig. 1(b). Due to hydrophobic property of PVP gate dielectric, microstructure of pentacene was bigger than bilayer dielectric.

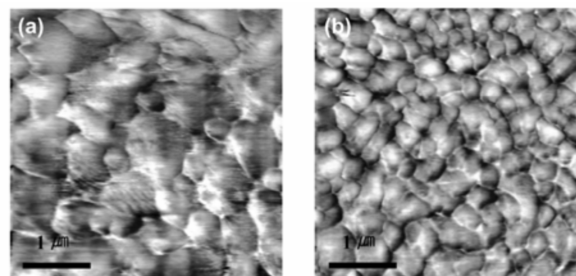

Figure 1. Atomic force morphology analysis : (a) pentacene on 450 nm PVP layer and (b) pentacene on HfO_2(10 nm)/PVP(450 nm) layer with electroplated Ni gate electrode on polyimide substrate.

Fig. 2 illustrates the plot of the drain current, I_{DS}, versus drain voltage, V_{DS}, at different gate voltage, V_{GS}, of the OTFT device with the 60 ㎛ channel length using the organic gate dielectric layer only. The transistor in Fig. 2 exhibited the mobility of 0.4 cm^2/Vs and the current on/off ratio, $I_{on/off}$, of ≅ 10^3.

Fig. 3 illustrates the plot of the drain current, I_{DS}, versus drain voltage, V_{DS}, at different gate voltage, V_{GS}, of the OTFT device with the channel size of 60 ㎛ using the PVP/HfO_2 bilayer gate dielectric. When compared with the OTFT with only PVP dielectric layer, the $I_{on/off}$ was increased to ≅ 10^5.

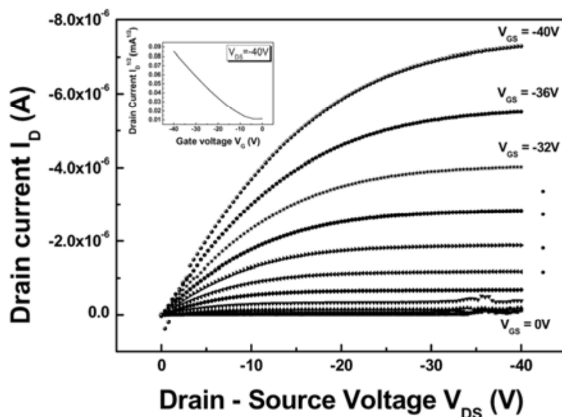

Fig. 2 Output characteristics of a fabricated OTFT wth the 450 nm PVP gate dielectric and channel length of 60 ㎛. The V_{GS} is swept from 0 to -40 V in steps of -4 V.

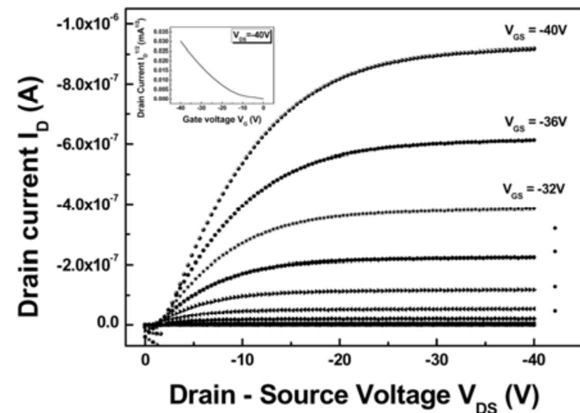

Fig. 3 Output characteristics of a fabricated OTFT with the HfO_2(10-nm)/ PVP(450 nm) gate dielectric and channel length of 60 ㎛. The V_{GS} is swept from 0 to -40 V in steps of -4 V.

The enhanced $I_{on/off}$ value in the present experiment is presumably attributed to the reduced off-current due to the reduced leakage current in the gate dielectric layer. I-V measurements of the PVP/HfO_2 bilayer capacitor with the metal electrode area of 150 x 150 μm^2 fabricated on the Si wafer showed that the leakage current was decreased from 6.5×10^{-8} A to 2.1×10^{-11} A at the electric field of 1 MV/cm, compared to the PVP capacitor.

However, the mobility was decreased to 0.07 cm^2/Vs due to reduced grain size of pentacene because HfO_2 surface has larger hydrophilic property than PVP surface. Surface energy of dielectric significantly affects the growth condition of pentacene [4,5]. In order to increase grain size of pentacene, surface treatment such as self-assembled monolayer may be necessary.

3. Conclusion

We fabricated flexible OTFT device using organic/inorganic bilayer gate dielectric with electroplated gate electrode. The current on/off ratio was significantly increased for the bilayer gate dielectric compared to PVP gate insulator. We found that application of low-temperature ALD HfO_2 layer on the PVP organic layer as a high-*k* dielectric is useful in improving the electrical performance of the OTFT device by reducing the leakage current of the gate dielectric layer.

4. Acknowledgments

This work was supported through the Korea Science and Engineering Foundation (Grant No. 2005-0563-000) and in part through the Center of Excellence program of the Korea

Science and Engineering Foundation (Grant No. R-11-2000-086-0000-0).

5. References

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