Fabrication of excimer laser annealed poly-Si thin film transistor using polymer substrates

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Abstract

In this paper, the characteristics of polycrystalline silicon thin-film transistors (poly-Si TFTs) fabricated on polymer substrates are investigated. The a-Si films was laser annealed by using a XeCl excimer laser and a four-mask-processed poly-Si TFT was fabricated with fully self-aligned top gate structure. The fabricated nMOS TFT showed field-effect mobility of ~30 cm^2/Vs, on/off ratio of 10^5 and threshold voltage of 5 V.

1. Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) fabricated at a low temperature process have been investigated to realize active-matrix liquid crystal displays (LCDs) with integrated drivers on large glass substrates [1]. Mass production of these TFT-LCDs began several years ago. The focus of current research is on new applications for low-temperature processed poly-Si TFTs. Low-temperature processed poly-Si TFTs are thought to have tremendous potential to realize other displays besides LCDs.

Plastic substrates are suitable for these applications because of their light weight, thin thickness, flexibility, robustness, and low production cost. The properties of typical plastic film substrate are summarized and compared with those of glass in Table 1. Plastic substrates are more robust than glass substrates due to their higher durability for bending. Therefore, application of thin film plastic substrate with low density can be expected to result in a display module that is about one order of magnitude lighter than one employing glass substrate.

Table 1. Comparison of the characteristics of polymer and glass substrates.

	T_g(℃)	CTE (ppm/K)	Resistivity (Ωcm)
PET	76.5	79.2	2×10^{15}
PC	150	70.2	7.3×10^{16}
PES	228	49.1	2.9×10^{16}
PEN	200	23	2×10^{17}
PI	385	20	1.5×10^{17}
Polyarylate	330	50	1.0×10^{16}
Glass(1737)	620	5	-

Recently, poly-Si TFTs directly fabricated on plastic films have been introduced to reduce the maximum process temperature to below 200°C [2][3]. A few years ago, D. P. Gosain et al. reported ULTPS TFT with field effect mobility as high as 250 cm^2/V·s on a polyethersulfone (PES) substrate while keeping the maximum process temperature under 110°C [3]. N. D. Young et al. [4] also reported nMOS and pMOS TFT on various polymer substrates with mobility up to 100, 52 cm^2/V·s respectively.

Electronic devices that are light weight, robust, flexible, and thinner can be anticipated if that is actually accomplished. However, practical devices such as TFT-LCDs have not been demonstrated yet, and it is obvious that several problems exist in the present processes to fabricate TFTs on plastic films. First, TFT performance tends to degrade when the maximum process temperature is reduced because of the difficulty of forming high quality films for gate insulators and channel silicon layers at low temperature, a fact that results in the diminution of the advantages of low-

temperature processed poly-Si TFTs. Second, mask alignment in the photolithography process is made more difficult due to the expansion of plastic film, a fact that will decrease yield and limit the scaling down of TFT size. Third, the handling of plastic film is completely different from that of glass substrates, and chemical treatments are also limited for plastic film. Therefore, it is impossible to use glass substrate and plastic film in the same processes and facilities.

2. Experimental

In order to minimize the stress induced during the fabrication process, the substrates should be pre-annealed before any inorganic material deposition step. Here the substrates were annealed at 180°C (for PES) or 250°C (for PAR; polyarylate) in a vacuum oven before the fabrication.

We begin with a substrate material of 200 μm-thick plastic substrates, a material similar to common overhead transparency sheets, chosen for its optical and chemical properties. A 650 nm-thick SiO_2 layer is deposited onto the plastic using Electron Beam evaporator at 100°C. This layer serves as a thermal barrier to protect the plastic during laser processing and to provide a smooth surface for deposition of subsequent layers.

Because a-Si films are brittle and withstand only quite limited strains, performance degradation of devices may occur from cracks or deformations created during the deposition and device fabrication process. Consequently, to minimize the residual stress induced in the Si film a counter layer must be deposited on the back side of the substrate. We applied various multilayer structures such as organic/inorganic hybrid buffer layers. For simple poly-Si fabrication, same thicknesses of SiO_2 layers were deposited on the both sides of the substrate to maintain the flatness of the film. However, in the case of TFT fabrication, different structure is needed due to the complexity of the TFT device.

Figure 1 shows the atomic force microscopy (AFM) topography of the SiO_2/plastic stack. Average surface roughness is measured about 1.07 nm.

The a-Si film was coated by sputtering in argon/helium mixture gas. The argon impurity concentration in the a-Si film was controlled by adjusting the argon/helium mixture ratio and working pressure.

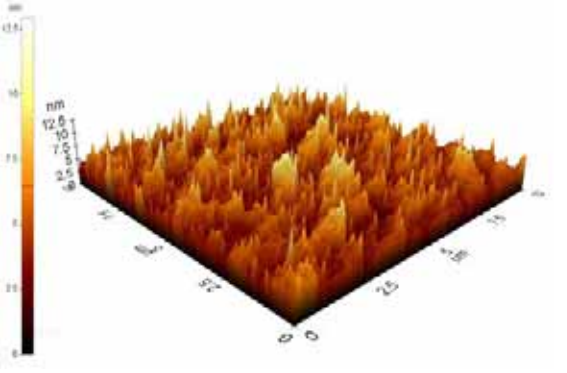

Fig. 1. AFM image of the SiO_2/plastic stack.

Figure 2 shows the AFM topography of the Si/SiO_2/plastic stack. Average surface roughness is measured about 0.89nm.

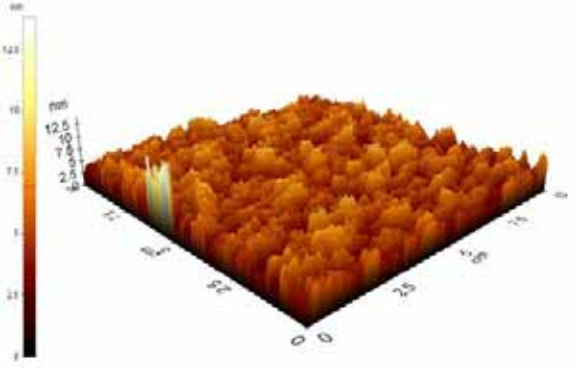

Fig. 2. AFM image of the Si/SiO_2/plastic stack.

The a-Si film was then laminated onto a glass substrate using a thin adhesive film and irradiated by XeCl excimer laser (λ=308 nm). The pulse duration and the beam size of the laser were 35 ns and 45 x 0.2 mm^2, respectively. After defining AlNd gate electrode (sputter, 200 nm) and gate insulator (sputter, 200 nm), ion shower process was carried out to dope the Si layer and activation was done again by laser. Then 400-nm-thick interlayer dielectric was deposited and contact hole was defined. Finally, 300-nm-thick AlNd source and drain electrode was deposited and patterned.

3. Result and discussion

As stated above, one of the disadvantages of using polymer substrates instead of using glass is the large shrinkage rates during thermal cycling process. In order to reduce the effect of irreversible shrinkage during TFT fabrication, the substrates must be annealed before the process starts. Figure 3 shows the shrinkage rates of PES substrates with various annealing conditions. The shrinkage rates were noticeably decreased with annealing time more than 60 hours. For PES substrates, the rates decreased from 180 ~ 200 ppm/K to 2 ppm/K, which is in the acceptable range for TFT fabrication process.

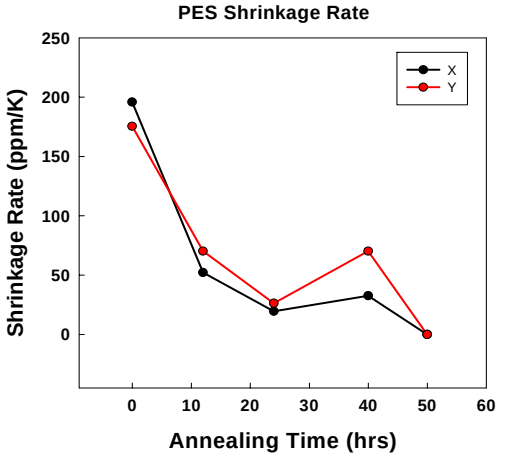

Fig. 3. Shrinkage rate changes of PES substrates as a function of annealing time.

Fig. 4. Image of poly-Si TFTs fabricated on a polymer substrate.

Electrical performance of the TFTs produced by process flow was checked with a semiconductor parameter analyzer after the fabrication of poly-Si TFTs using sputter deposited a-Si precursor films.

Figure 4 shows the TFT transfer characteristics (I_d-V_g). The calculated field-effect electron mobility calculated from the TFT device characteristics in the linear region was 30 $cm^2/V{\cdot}s$, on/off ratio of 10^5 and threshold voltage of 5 V.

A summary of the electrical parameters of TFTs fabricated at a substrate temperature of 110°C is given in Table 2.

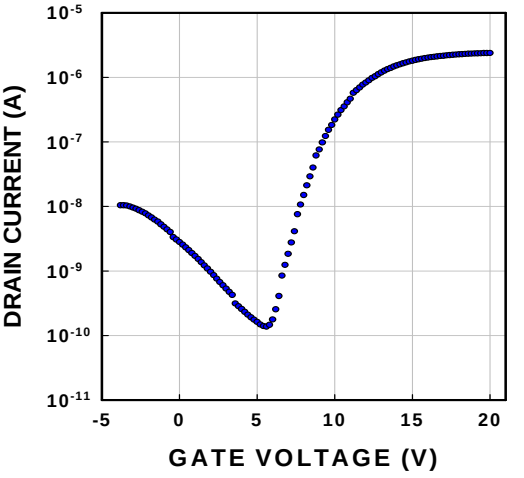

Fig. 5. Transfer characteristics of fabricated nMOS poly-Si TFTs on polymer substrates.

Table 2. Electrical properties of a poly-Si TFT device fabricated on a plastic substrate.

Parameter	Value
Mobility	30 $cm^2/V{\cdot}s$
on/off	10^5
Vth	5V

5. Conclusion

We have showed that poly-Si can be obtained using excimer laser crystallization of sputtered films on a plastic substrate. We have developed a process suitable for TFT fabrication on plastic. Poly-Si TFTs with a mobility of 30 $cm^2/V{\cdot}s$, threshold voltage of 5 V and an on/off ratio of more than 10^5 were fabricated on a plastic substrate at a process temperature of 110°C.

The sputter deposition has the advantages of low process temperature and low impurity concentration, suitable for the fabrication of flexible active-matrix type displays with integrated driving circuits.

6. References

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