Plasma Oxidation Effect on Ultralow Temperature Polycrystalline Silicon TFT on Plastic Substrate

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Abstract

The TFT performances were enhanced and stabilized by plasma oxidation of the polycrystalline Si surface prior to the plasma enhanced atomic layer deposition of Al_2O_3 gate dielectric film. We attribute the improvement to the formation of a high quality oxide interface layer between the gate dielectric film and the poly-Si film. The interface oxide has a predominant effect on the TFT's characteristics, and is regulated by the gap distance between the electrode and the polycrystalline Si surface.

1. Introduction

Flexible displays are currently the subject of a great deal of interest due to their low weight, superior compactness, robustness and design flexibility compared with conventional glass-based displays. In order to realize a mechanically stable display, however, several issues must be resolved [1].

Inorganic materials have very different mechanical properties compared with plastic substrates; therefore, cracking and delamination may occur during the fabrication process and in operation. Furthermore, the thermal expansion coefficients of plastic substrates are much larger than those of inorganic materials and consequently, stresses during the deposition process are introduced. If a freestanding substrate is employed, the curvature of the inorganic film structures on plastic substrates changes during circuit fabrication, causing misalignment between the layers.

In order to prevent this misalignment, the plastic substrate is typically bonded to a rigid carrier. The adhesive used for bonding must withstand the TFT process temperatures and chemicals; therefore, the use of an adhesive necessitates a reduction of the maximum process temperature from the value that the substrate itself would normally withstand. The aforementioned issues as well as the low thermal resistance of most plastic substrates necessitate an ultra low temperature poly-Si (ULTPS) TFT process [2-6].

The crystallization of sputter deposited a-Si films was achieved by either excimer laser annealing [2-5] or sequential lateral solidification (SLS) [6,7]. Recently, we have reported on a successful SLS on a plastic substrate that yielded micron size large grain poly-Si films [8]. To prevent damage on the plastic substrates during the laser dopant activation, a quarter wavelength Bragg reflector, made by successive depositions of plasma-CVD silicon dioxide and silicon nitride film [5] and the oxide-silicon-oxide (SiO_2-Si-SiO_2) buffer structure [9], was suggested.

For gate dielectrics, the chemical vapor deposition SiO_2 [2,4-6], sputter deposition SiO_2 [4] and plasma enhanced atomic layer deposition (PEALD) Al_2O_3 films [7,10-12] have been reported. A two-layer gate insulator composed of a thermal or plasma oxidized SiO_2 and PEALD Al_2O_3 on silicon substrate [7,10] shows high quality characteristics. Because the plastic substrate on the thin carrier (silicon of 0.6 mm thick) was easily deformed during thermal processing, it is necessary to process the plastic substrate on a thicker carrier (glass of 1.1 mm thick).

The TFTs fabricated on the plastic substrate with a glass carrier [9] do not show the high quality characteristics which was observed on the silicon substrate [10] or on the stainless steel foil [11]. Aiming to improve and ultimately realize TFTs on plastic substrates, we focus on the interface between the poly-Si and Al_2O_3 formed by the PEALD.

2. Results

The buffer structure is designed to have an absorption layer sandwiched between the buffer oxide films [9]. Because a-Si film as an absorption layer effectively absorbs the laser light during the dopant activation process using a laser, the plastic substrate is protected.

After laminating the plastic substrate on a glass wafer, we sputtered a buffer oxide I layer of 250 nm thick SiO_2 film on the plastic substrate using RF-magnetron sputter deposition method at 300 W and 0.15 Pa.

Subsequently, we deposited an 80 nm thick a-Si film for an absorption layer at RF power of 1 kW and Ar pressure of 0.48 Pa. Then, a buffer oxide II of SiO_2 film was deposited on the absorption layer using RF-magnetron sputter deposition method at 300 W and 0.15 Pa.

Due to the thermal restrictions, ULTPS-TFT processes have met difficulties in annealing the interface between channel and the gate dielectrics. We tried to oxidize the Si surface with pulsed O_2 plasma at a condition of 300 W for 30 min before the Al_2O_3 deposition by PEALD.

Prior to the oxidation, the surface of the Si substrates was cleaned with a 100:1 hydrofluoric acid solution to remove the native oxide layer.

We have varied the gap distance between the electrode and the sample surface to observe the effect on the TFT performance. Usually, to facilitate the transport of reaction gas species, PEALD uses a narrow gap distance [14]. The Si surface was cleaned to remove the native oxide layer. The working conditions were set to produce 50 nm thick Al_2O_3 layers with prior plasma oxidation at 180 ^oC.

Figure 1 shows transmission electron microscopy (TEM) images of SiO_x/Al_2O_3 interfaces with gap distance variation. The interface gains thickness upon increasing gap distance.

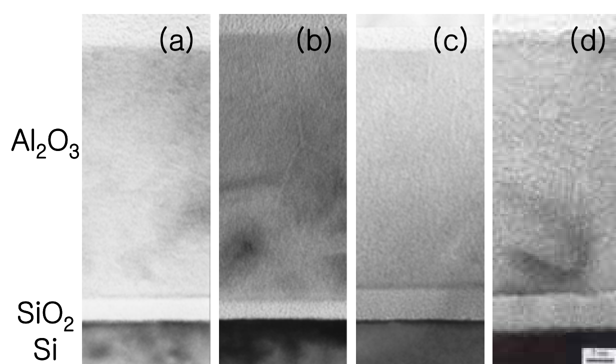

Figure 1. Transmission electron microscopy images of interface layer, SiO_x, and Al_2O_3 layer with a gap distance variation both in the plasma oxidation and in the 50 nm Al_2O_3 deposition. (a) 3.0 mm, (b) 3.6 mm, (c) 4.2 mm, and (d) 4.8 mm.

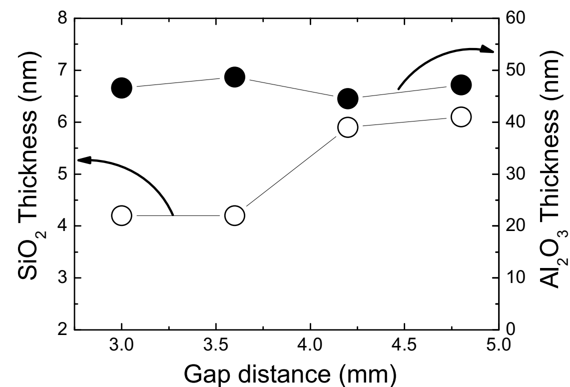

Figure 2. Thickness variation of SiO_x and Al_2O_3 layer with the gap distance obtained from TEM observation.

The result of fig. 1 was quantitatively analyzed in fig. 2. As can be seen, the SiO_x layer thickness is rather insensitive up to gap distance of 3.6 mm, and then increases significantly up to 4.2 mm. The Al_2O_3 layer thickness do not vary with the gap distance.

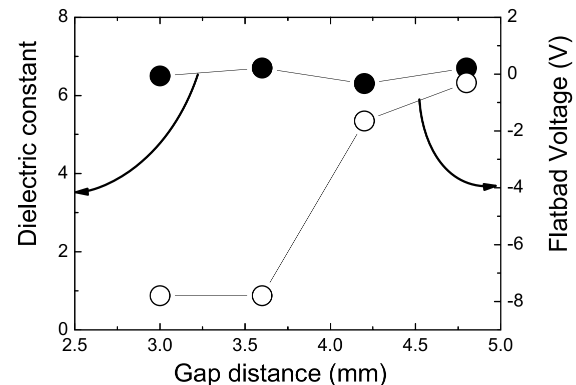

Figure 3. Changes in the dielectric constants and flatband voltages of 50 nm grown gate dielectric with a gap distance variation using C-V measurement.

Figure 3 shows the changes in the dielectric constants and flatband voltages of 50 nm thick gate dielectric with a gap distance variation using C-V measurement. Apparently, the dielectric constants show no explicit dependency on the gap distance. However, the

flatband voltages approach zero voltage as the gap distance is increased.

Figure 4 shows the transfer characteristics of the nMOS and pMOS TFTs fabricated at 180 ^{o}C on plastic substrates. Al_2O_3 gate dielectric was grown (a) at a 4.0 mm and (b) at a 3.3 mm gap distance. The high performances of the nMOS/pMOS TFTs with mobilities of 154 and 33 cm2/Vs, threshold voltages of 5.8 and -7.3 V and sub-threshold swings of 1.0 and 0.78 V/dec, respectively, were obtained at a 4.0 mm gap distance while poor performances were obtained at a 3.3 mm gap distance.

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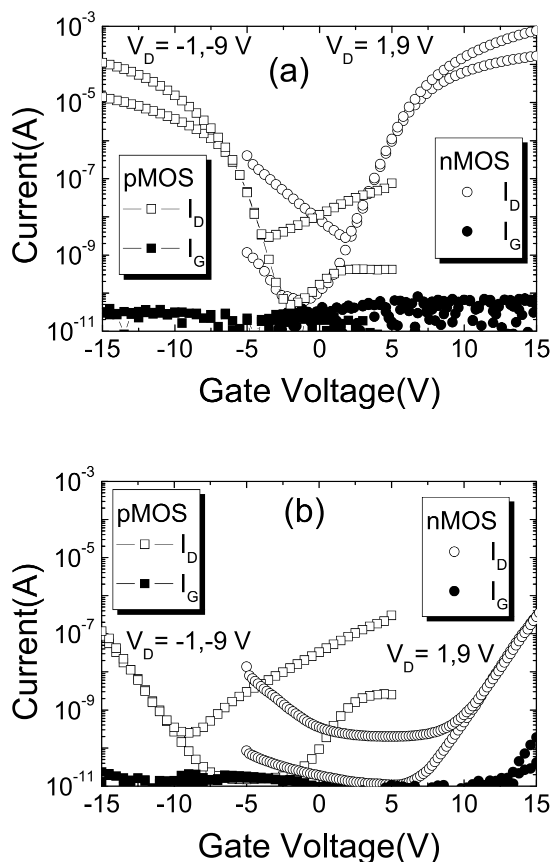

Figure 4. Transfer characteristics of the nMOS/pMOS TFT fabricated at 180 ^{o}C at (a) 4.0 mm and (b) 3.3 mm gap distance.

3. Conclusion

The TFT performance was enhanced with increasing the gap distance in the PEALD process for dielectric deposition. We attribute this to the formation of a high quality oxide interface layer between the gate dielectric film and the poly-Si film.

4. Acknowledgements

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5. References

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