Computer Generation of Equivalent Circuit for Unit Cell of LCD-TV

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Abstract

In this paper, we propose a method for automatic generation of equivalent circuit for unit cell of LCD-TV. In order to extract a circuit model, computer program generates electrical connectivity of resistors and capacitors from the layout through pattern analysis with electrode and port information. For combining two types of independent equivalent circuits, we propose a node insertion algorithm. As a consequence, we can generate an equivalent RC circuit without increasing the capacitive elements.

1. Objectives and Background

Recently, since the resolution and color depth of LCD panel are increasing as well as its size, the industry standard in LCD-TV requires that the gray level voltage should be controlled within ±2mV in order to guarantee the accuracy in 10-bit gray scale [1]. However, the time for row line scanning tends to shrink while resistive and capacitive loads at the gate and data bus lines increase. Therefore, an accurate pre-analysis on the electrical properties of bus lines in the LCD-TV panel is critically important at the design and verification stage of a unit pixel.

In order to verify the electrical properties of LCD panel, the extraction of equivalent circuit for unit cell of LCD panel is strongly needed. Therefore, in this paper, we propose a compact modeling approach based on a rigorous calculation of electric field in the panel area.

2. Automatic Generation of Equivalent Circuit

Figure 1 shows a schematic diagram illustrating the workflow of the proposed scheme. Referring to figure 1, our approach is comprised of the following steps:

1) Importing GDSII standard layout file;
2) Adding electrical information to the layout and defining process recipes;
3) Generating 3D mesh structure from the layout and process recipe given in step (2);
4) Calculating parasitics based on three-dimensional electric-field calculations;
5) Performing pattern analysis with the electrical information given in step (2) in order to generate an electrical connectivity; and
6) Generating equivalent circuit model based on the electrical connectivity with the calculated parasitics and additional TFT model information.

In order to calculate the electric-field, we have solved the Ericksen-Leslie's equation and two types of Laplace's equation in the dielectric and conductor domain by the finite element method, respectively. Furthermore, we have used the energy method which calculates capacitance and resistance values from the electric-field energy stored in the dielectrics and the power loss in the conductors [2]. In order to define boundary conditions for calculating resistance and capacitance and generate electrical connectivity, two types of information, electrode and port information are needed.

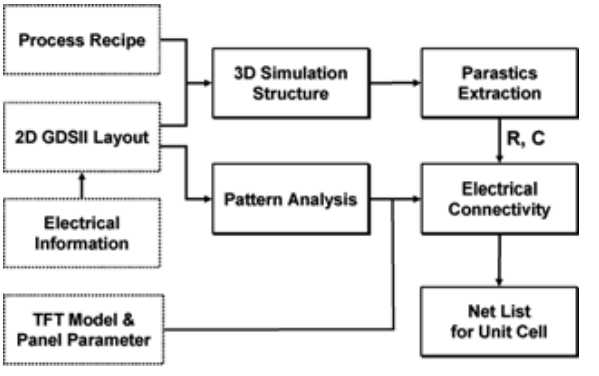

Figure 1. Schematic diagram illustrating the work-flow for extracting net-list.

The electrode information means the name of an electrode wherein the electrode information includes all the electrode conductors that are electrically connected. Moreover, the electrode information is referred when the boundaries should be defined for the calculation of the electric-field in the dielectric domain and the conductor domains are needed to be defined for the calculation of resistance. The port information is the name of port and position which are used to define boundaries for the calculation of the electric-field in the conductor domains.

In order to generate equivalent circuit model, each electrode and port is transferred into electrical node of equivalent circuit. n electrodes can be modeled as ${}_nC_2$ capacitors and each electrode modeled as the resistors by its port information. In the case of the electrode containing m ports can be modeled as ${}_mC_2$ resistors similar to the case of the capacitors. Specially, an electrode which has no port information is considered as the electrical node only. Figure 2 shows a schematic view of an exemplary layout, its 3 kinds of equivalent circuit.

Referring to figure 2(a), the exemplary layout includes 3 electrodes which have 2 ports (1, 2 in A), 0 port, and 3 ports (3, 4, 5 in C), respectively. Referring to the resistive and capacitive equivalent circuits as show in figure 2(b) and (c), the electrode A was transferred into 1 resistor and the electrode C was transferred into 3 resistors, and 3 electrodes were transferred into 3 capacitors.

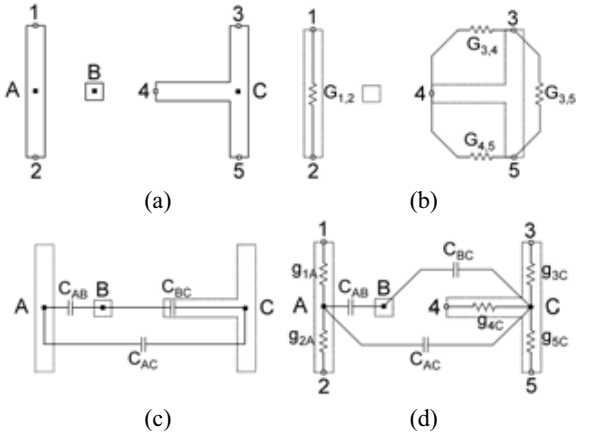

Figure 2. (a) Exemplary layout and its (b) resistive, (c) capacitive and (d) the combined equivalent circuit.

However, since resistance and capacitance have been calculated independently, the resistive and capacitive equivalent circuit should be combined for next circuit simulation. In order to combine resistive and capacitive equivalent circuit, the number of parasitic capacitance is increasing.

Therefore, we have proposed node insertion algorithm to generate the RC-merged equivalent circuit without increase of the number of capacitance. The proposed node insertion algorithm is based on node elimination [3]. Figure 3 shows a schematic view illustrating the rule of the node elimination for resistive elements. Referring to figure 3, conductances g_{mi} and g_{ni} can be merged into g_{mn}, and g_{mn} is described by Equation (1) [3].

$$g_{mn} = g_{mi} g_{ni} / \sum_{k=1}^{p} g_{ki} \qquad (1)$$

From equation in figure 3, the resistive and capacitive equivalent circuits shown in figures 2(b) and (c) can be combined as shown in figure 2(d).

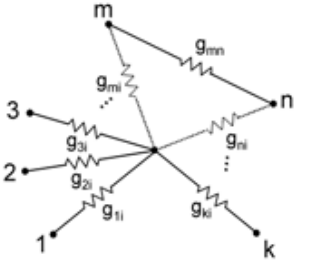

Figure 3. Schematic view illustrating the rule of node elimination for resistive elements.

3. Applications

In this work, we have applied our method to the exemplary unit cell. Furthermore, a graphical input interface was developed to generate equivalent circuit automatically from the layout of unit cell. Figure 4 illustrate the layout of exemplary unit cell and its 3D structure. Referring to the figure 4, the layout includes a total of 7 electrodes and 14 ports comprising two gate lines, two data lines, storage, pixel, and common electrodes. Furthermore, each one of data and gate lines, storage and pixel electrodes are including two

ports, respectively, while another one of data and gate lines are including three ports and common electrodes is including no port. Therefore, the layout of unit cell can be modeled by 10 resistances, 21 capacitances, and a TFT. We have used our FEM numerical solver to calculate the resistances and capacitances, and the calculated values were stored according to the convention of SPICE net-list for next-step circuit simulation and analysis. Figure 5 shows schematic view of the equivalent circuit of unit cell with some major parasitic elements.

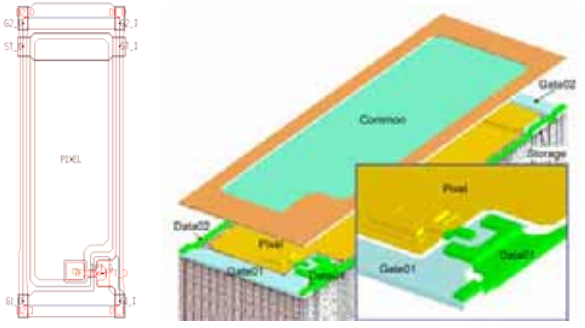

Figure 4. Exemplary unit cell and its 3D structure.

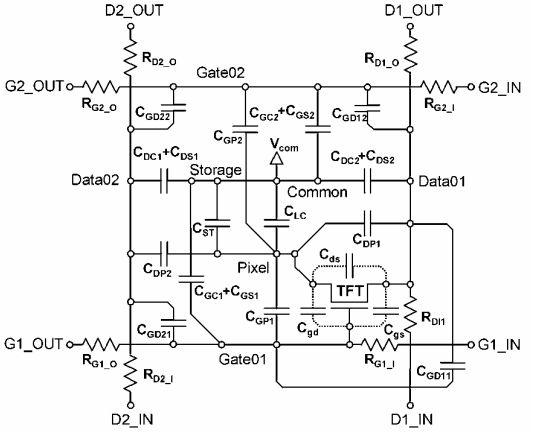

Figure 5. Equivalent circuit of the exemplary unit cell.

Figure 6 is an original reference image with 1366×768 size having 8-bit color. The image quality of Figure 6 is HDTV while the gray-level of R, G, and B is 256. From the reference image shown in Figure 6, a gray-level was extracted from the V-T curve and a gamma correction curve. In this work, it is assumed that the gate line resistance for the worst case simulation was chosen to be 19.2 ohms. Figure 7 exhibits the simulated image taking into account all the resistance and capacitances in the model for the worst case.

Figure 6. Original reference image with 1366×768 size having 8-bit color.

Figure 7. The simulated image taking into account all the resistance and capacitances in the model for the worst case.

Figure 8. The simulated image when the gate line resistance is 3.2 ohms with keeping other parameters unchanged.

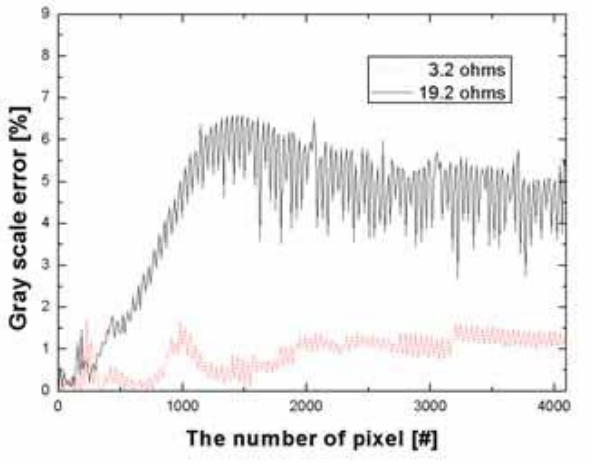

Figure 9. Schematic diagram illustrating the fluctuation caused by crosstalk.

In this simulation, the frame inversion by column was assumed. The gate voltage ranges from -6 to 30 V while the data voltage varies between 0 and 14 V. The kick-back voltage was calculated to be 0.35 V and the common voltage was set 6.5 V. Referring to Figure 7, we can observe the shading effect and gray scale error induced by gate line delay in the simulated image of the panel. Furthermore, a vertical line crosstalk induced by driving with column line inversion is visible if we take a careful look at the simulated image. In Figure 7, the gray scale error is clearly depicted from the 520-th pixel to the last pixel, which seems to be due to the gate line delay.

Figure 8 exhibits a simulated image when the gate line resistance is to be 3.2 ohms with keeping other parameters unchanged. Referring to Figure 8, vertical line crosstalk and gray scale error seem to be alleviated with comparison to the image illustrated in Figure 8. The simulation reveals that the image quality can be adjusted either by the magnitude of the metal line or the species of material of the row-line interconnection, as mentioned earlier. As the number of pixel is increased, the gray scale error tends to be more pronounced due to the fact that the worst case panel has a greater gate line resistance than the improved panel. In Figure 9 is shown a schematic diagram illustrating the fluctuation caused by crosstalk.

4. Conclusion

In this paper, we have proposed a method for automatic generation of equivalent circuit for unit cell of LCD-TV. In order to extract a circuit model of unit cell, we generated electrical connectivity of resistors and capacitors from the layout automatically by pattern analysis with electrical information comprising electrode and port information. In order to combine two type of independent resistive and capacitive equivalent circuit, we proposed node insertion algorithm. Thereafter, we calculated the parasitic elements by energy method with FEM. The output parasitics were stored according to the convention of SPICE net-list.

5. Acknowledgements

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6. References

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