Development of Electrical Models of TFT-LCD Panels for Circuit Simulation

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ABSTRACT

As the film transistor-liquid crystal display (TFT-LCD) panels become larger and provide higher resolution, the propagation delay of row and column lines, the voltage modulation of Vcom, and the response time of liquid crystal affect the display images now more than in the past. It is more important to understand the electrical characteristic of TFT-LCD panels these days. This paper describes the electrical model of a 15-inch XGA (1024×768) TFT-LCD panel. The parasitic resistance and capacitance of its panel are obtained by 3D simulation of a sub pixel. The accuracy of these data is verified by the measured values in an actual panel [1]. The developed panel simulation platform, the equivalent circuit of a 15-inch XGA panel, is simulated by HSPICE. The results of simulation are compared with those of experiment, according to changing the width of $\overline{\text{OE}}$ *signal. Especially, the proposed simulation platform for modeling TFT-LCD panels can be applied to large size LCD TVs. It can help panel and circuit designers to verify their ideas without making actual panels and circuits.*

1. Background and History

Cathode-Ray Tubes (CRT) have been replaced with flat panel display (FPD) devices such as a TFT-LCD panel and a plasma display panel (PDP) in monitor and television markets these days. The thickness of FPDs is not proportional to their screen size. This is the great advantage of FPD devices. Among FPDs, a TFT-LCD is emerging as the most leading device in HDTV markets.

However, TFT-LCDs should overcome several barriers to succeed in these markets. These barriers are lower contrast ratio, less bright, slower response time, poorer viewing angle, worse color reproduction than CRT TVs. For example, as the TFT-LCD panels becomes larger and provides higher resolutions, it is more important to consider the propagation delays of row (gate) and column (data) lines and the fluctuations of vcom voltage. As a result, they deteriorate the charged voltage in each pixel and affect the display image. To overcome them, a lot of technologies are implemented to improve the performance of TFT LCD. Finally, LCD TVs are competitive to CRT TVs. However, we should still improve the quality of images in LCD TVs. Therefore we approach these issues from the system level. When we design new TFT-LCDs, we should consider the characteristic of panels and circuits. To realize that, it is essential to develop the electrical equivalent model of TFT- LCD panels.

The architecture of the equivalent model of TFT-LCD panels is described in section 2. Section 3 explains the implementation of the simulation platform of 15-inch XGA (1024×768) TFT-LCD panel based on the results of measurement and 3D simulation extracting parasitic capacitances and resistors [1]. The simulation results of this panel simulation platform are compared with the measurement results by changing $\overline{\text{OE}}$ in section 4. Finally, the conclusion and the impact follow in section 5.

2. The Equivalent Model of TFT – LCD Panels

LCD panels can be modeled by resistors and capacitors like Figure 1.When row (gate) and column (data) line signals propagate through each line to the other side of panel, they are delayed by resistance and capacitance in each line. Each row and column line should be together with vcom, common electrode. Vcom is made of ITO (Indium Tin Oxide). It is not a perfect conductor and has resistance. Therefore, Vcom model should be made to consider voltage changes of neighboring pixels. Figure 1 is drawn in view of equivalent circuits according to voltage and current. Except for line models and vcom model, the electrical

model of TFT LCD panel should have TFT and LC model.

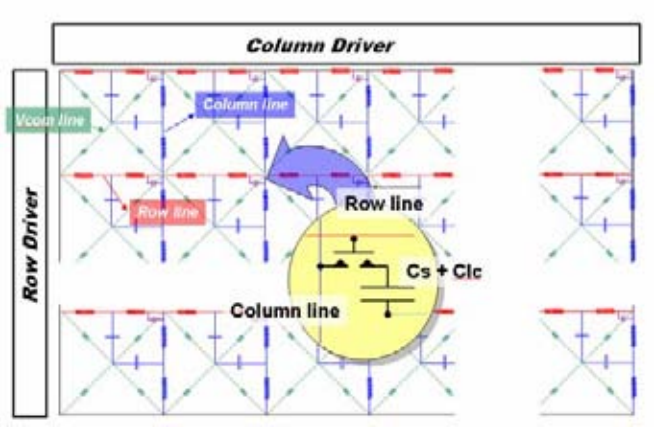


Figure 1 The simplified TFT-LCD panel

Models of these five components, a row line, a column line, a TFT model, a LC model, and a vcom, are necessary to explain operation of a TFT-LCD panel. All parasitic resistance and capacitance are obtained by the 3-dimensional parasitic extraction simulation tool after observing a real unit pixel, drawing a 2 dimensional and a 3 dimensional structure like Figure 2. All electrical models are verified by comparing the simulated data and measured data in actual 15-inch TFT LCD panels [2]. Table 1 illustrates electrical models of each component in the equivalent model of TFT-LCD panels.

Table 1 Electrical Models of Each Component

Component	Model
Row(Gate) line	RC Distributed Line Model(16)
Column(Data) line	RC Distributed Line Model(12)
TFT(Thin Film Transistor)	HP TFT Model
Liquid Crystal	Behavioral Model Using VCCAP
Vcom	Modifying Ground Plane Model

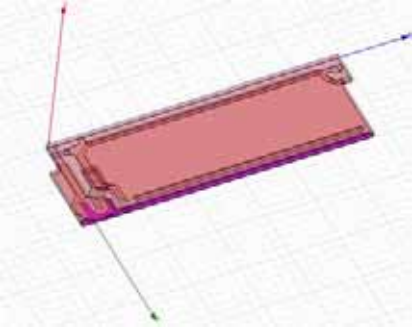


Figure 2 3-dimensional structure of a sub pixel

2.1. A RC Distributed Row/Column Line Model

The row/column line in TFT-LCD panel can be modeled by RC distributed model. The lumped RC model is pessimistic and inaccurate for long interconnect wires [4]. If unit pixel in 15-inch XGA (1024×768) panel is one lumped T model, one row (gate) line consists of 6144 (=1024×3×2) resistors and 3072 (=1024×3) capacitors. There are 1536 (=768×2) resistors and 768 capacitors in column (data) line. Since the time-constant grow with the length [13], we have to consider the distributed model which is composed of several lumped models. It is needed to research how many blocks (N) are acceptable and accurate.

As shown in Figure 3, row/column line can be considered as the distributed model which is made up of N blocks. The bigger number N has, the closer waveform from this model becomes to the real waveform. But it is not necessary for block to be divided by 1024 in gate line and 768 in data line. The optimized distributed model can be found out through HSPICE, increasing N.

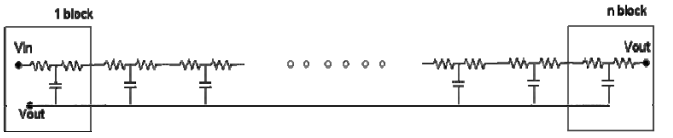


Figure 3 N-Distributed T model

After Increasing N, the number of T model, we got the optimized number of N in row and column line case. N_{row}, the optimized number in a row line, is 16. N_{column}, the optimized number in a column line, is 12

2.2. A TFT Model

A lot of researches on TFT have been done. The representative TFT models are the HP model [2] and the RPI model. These models are supported in SPICE environment [3].We used level 40 HP a-Si model. Figure 4 illustrates I-V curves of the simulated result using HP model and the measured result in a TFT of a 15-inch TFT-LCD panel. It is shown that the simulated result fits the measured results well in operation region of TFT.

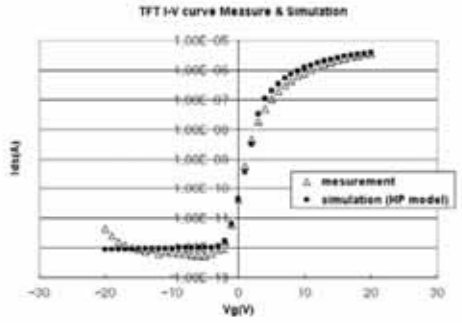


Figure 4 Comparison of the simulated result of HP model with the measured results (I-V curve)

2.3. A Liquid Crystal Behavioral Model

We can consider liquid crsystal (LC) as a dielectric material. The capacitance of liquid crystal is varied to the applied voltage and determined by the tilt angle and twist angle of the liquid crystal molecules. When the applied voltage varies, the liquid crystal molecules' tilt angle and twist angle varies. So, we can calculate the capacitance from the tilt angle and twist angle. But this method is very complicated and takes the large calculation time. It isn't a good model for the designers to use. Our behavior models focused on the variations of capacitance value across the voltage of the liquid crystal. We fitted the reference data about each LC material (Usually LC material companies provide it for TFT-LCD panel manufacturing companies). To implement the LC behavior model into TFT-LCD panel simulation platform, we have to use VCCAP (Voltage Controlled Capacitor) model in HSPICE [3].VCCAP can express the variation of capacitor according to the applied voltage. Considering a response time of LC, Low pass filter circuits should be inserted.

The LC behavioral model is designed in Figure 5. VCCAP is controlled by the voltage between +in and –in and capacitor is hung between drain (+out) and vcom (-out). Pixel voltage between drain and vcom is transferred to the voltage between B and vcom by dependent voltage source having that gain is 1.

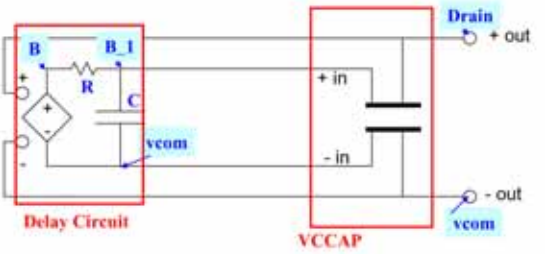


Figure 5 The LC behavioral Model

This voltage is delayed by a resistor and a capacitor. Even though capacitance changes immediately in VCCAP, capacitance of LC doesn't change immediately because of the control voltage between +in and –in already delayed. We used the highest relative dielectric constant of LC (=14.7) in 3D simulation and calculated the Area/Cell gap to get varying capacitance according to applied voltage, having a nonlinear characteristic. The LC behavioral model is implemented as texts in HSPICE environment. The response time of LC is determined by the RC time constant of the proposed LC behavioral model.

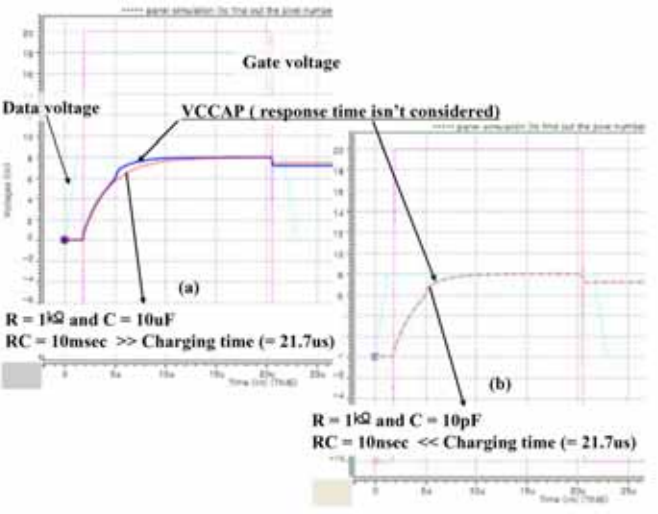


Figure 6 The simulation results (a) when C = 10 uF (b) C=10 pF

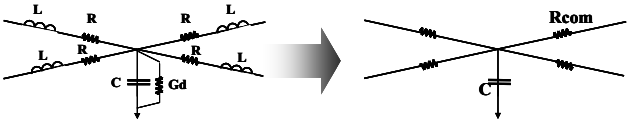
We used the schematic of TFT and applied the LC behavior model to it, and did simulation. After R(=1kΩ) is fixed, C is changed as 10uF and 10pF. Changes of the slope at the node were observed in Figure 6 (a) and (b). Figure 6 (a) shows that capacitance of LC doesn't change during charging time (21.7us). That is because this RC time constant (=10msec) is much longer than the charging time (=21.7 us). On the other hand, Figure 6 (b) shows that capacitance of LC changes immediately. Because the RC time constant (=10nsec) is much smaller

than the charging time, capacitance of LC changed immediately.

2.4. A Vcom Model

In TN LCD panels, a vcom plane is placed and deposited on a whole color filter part. The voltage of vcom is the reference voltage of the LCD panel. Therefore we can consider this plane as ground plane or power plane. The voltage of vcom fluctuates according to variations of gate and data voltage. It means that current go into or out of vcom. If vcom is made of a superconductor, its voltage won't fluctuate. This fluctuation makes horizontal crosstalks of LCD panels, because vcom connected every pixel. It is important to understand flowing of current and voltage in view of electrical properties in LCD panels.

We can consider that modeling vcom is the same as modeling power and ground plane in high speed digital system except for operating frequency [5]. Vcom is divided into square unit cells with lumped element models in Figure 7. The number of square unit cell in TFT-LCD panels is determined by the number of block in the distributed row and column lines. In this 15-inch XGA panel, there are 16-block distributed row lines and 12-block distributed column lines in Figure 8. The unit cell of Vcom represents 64(=768/12)×192(1024×3/16) sub pixels. The results of calculation are as follows:



R = Rdc + Rac = 34.54 + 5.88E-4 = 34.54 Ω
L = 5.82E-12(H) → can be ignored
C = value from 3D simulation
Gd = 9E-6 → can be ignored
(∵ Maximum frequency = 46kHz)

Figure 7 The Vcom Model

ρ = resistivity of ITO (Indium Tin Oxide), t = thickness of ITO

δ_s = skin depth of ITO at 46kHz, μ_o = permeability constant

d = Cell gap of LCD panel, w = the length of unit cell in row and column

C= the total capacitance between ITO and other layers

tan(δ)= loss tangent of dielectric

(This value is usually below 0.01 except for water.)

$$R = R(dc) + R(ac)$$

$$R(dc) = \frac{\rho}{t} \times \frac{w}{w} = \frac{190 \times 10^{-8}\,\Omega \bullet m}{550 \times 10^{-10}\,m} = 34.54\Omega$$

$$R(ac) = \frac{\rho}{\delta_s} = \frac{190 \times 10^{-8}\,\Omega \bullet m}{3.23 \times 10^{-3}\,m} = 5.88 \times 10^{-4}\,\Omega$$

$$L = \mu_0 \times d = (4\pi \times 10^{-7}\,H/m) \times (4.6um) = 5.8 \times 10^{-12}\,H$$

$$Gd = \omega C \tan(\delta) = (46 \times 10^3) \times (19563\,pF) \times (0.01) = 9 \times 10^{-6}\,\Omega^{-1}$$

C (Capacitance) uses the value that got from the 3D parasitic parameter extraction tool. It means that row, column lines, TFT, LC behavioral model are connected to the cross point, vcom. As we know the calculated results of each component, we can ignore R(ac), Inductance(L), Conductance(Gd). The final model vcom is shown in the right side of Figure 7. Rcom is 34.54 ohms, because the resistance values should be the same as each values every direction of unit cell block.

3. TFT-LCD Panel Simulation Platform

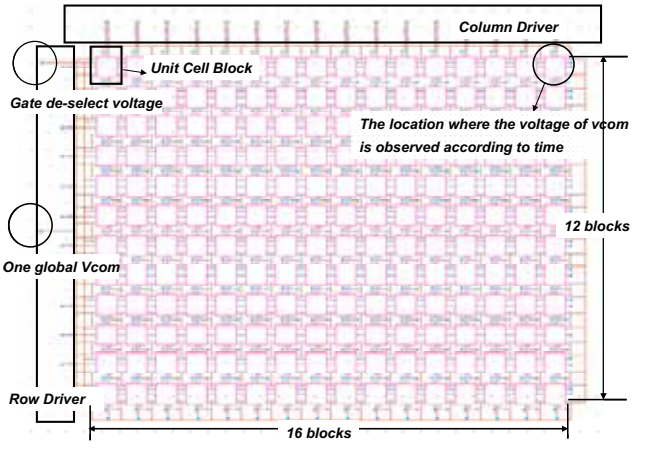


Figure 8 The Panel Simulation platform

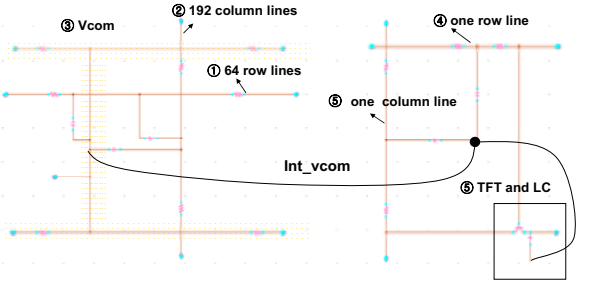


Figure 9 Unit Cell Block

We developed the 15-inch panel simulation platform in Figure 8. It is based on each electrical model in section

2. Column drivers and row drivers are also modeled in this simulation platform. It is possible to make any signals we want to drive and also connect the schematics of circuits. To make equivalent circuits, one unit block in Figure 9 is a lumped RC model representing 64 row lines and 192 (64*3) column lines together with a Vcom sheet. One row line, column line, TFT, and LC behavioral model are inserted into a unit cell block to observe a voltage of a pixel in every part of panels. These voltages of pixels are affected by RC delay of each line and variations of Vcom. Each resistance, capacitance, parameters of TFT, the characteristics of LC is changeable for every LCD panel of sizes and resolutions.

4. Results

There are a lot of possibilities to use this panel simulation platform. Among them, I will explain why the shortened gate pulse is used in the current TFT LCD industries. In XGA(1024*768) LCD panels, a theoretical one line time is about 21.7us (=1/60/768).Except for the charge sharing time (about 1us), the budget of one line time is about 20.7us. The shorten gate pulse is used because of RC delay of gate line. OE (Output Enable) signal is used to make the reduced gate pulse. The conditions of simulation are shown in Figure 10. We can see the results of HSPICE simulation, the variations of pixel voltage according to $\overline{OE}$ signal in Figure 11. As $\overline{OE}$ is getting smaller, a Gate on time becomes longer and TFT doesn't turn off immediately because of a delay of a row line. Figure 11 shows that the difference of pixel voltage in top right of the panel simulation platform between $\overline{OE}$ = 0us and $\overline{OE}$ = 3us is 0.74 V. This 15-inch TFT LCD has 64 gray levels and the difference of voltage between 0 gray and 63 gray is 4 V. Assuming that T(gray level) vs V(pixel RMS voltage) curve is linear, each gray level has 0.0625V. 0.74V is about 12 gray levels. This will affects image of TFT LCD. We can see the conversion results of HSPICE simulation through MATLAB in Figure 12. Figure 13 shows the results of measurement in a 15-inch TFT-LCD, the display images according to $\overline{OE}$. Comparing Figure 12 with Figure 13, the converted image using MATLAB reflect the measured image well. We can see change of display images into top right corner of this LCD panel. This simulation platf orm expresses a deterioration of image well.

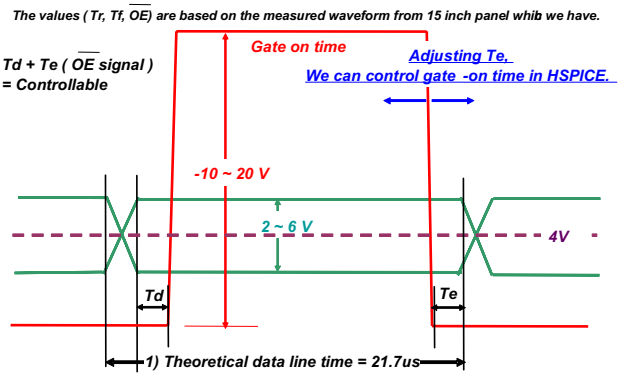


Figure 10 The simulation condition

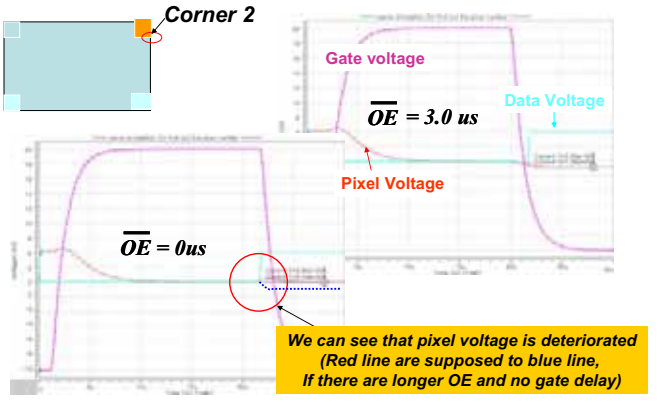


Figure 11 The pixel voltage according to $\overline{OE}$ in HSPICE simulation in top-right of 15-inch panel simulation platform

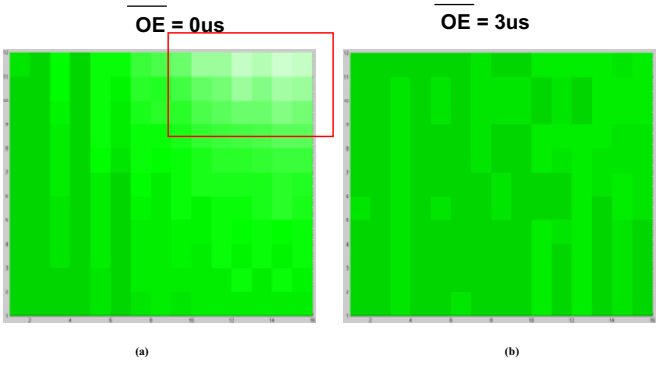


Figure 12 The conversion display images according to $\overline{OE}$ in HSPICE simulation of 15-inch TFT-LCD

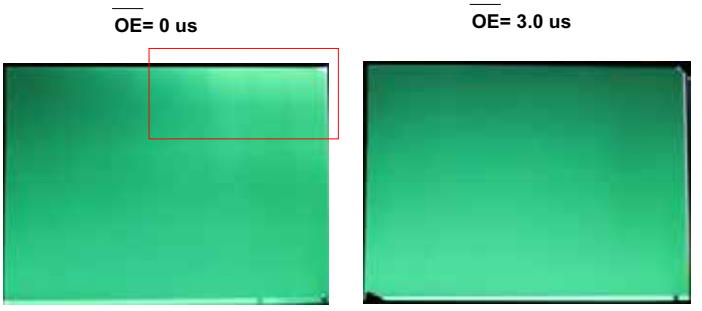


Figure 13 The display images according to $\overline{OE}$ in measurement of 15-inch TFT-LCD

5. Conclusion and Impact

We analyzed and developed electrical models of TFT LCD panels and the 15-inch panel simulation platform for SPICE simulation. Changing the value of each model suitable for any inch TFT-LCDs, we can develop the simulation platform for those TFT-LCDs. To improve the quality of image of TFT-LCD, engineer involved in LCD industry try to realize many ideas in various fields. However it takes long time to verify their ideas and it costs much. The panel simulation platform made in this paper will help a lot to verify them without making the real panels and circuits. It also save cost and time do it.

6. Acknowledgement

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