Effect of Density-of-States (DOS) Parameters on the N-channel SLS Poly-Si TFT Characteristics

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Abstract

The dependence of n-channel 2 shot SLS poly-Si TFT characteristics on the DOS (density of states) parameters was investigated by using a device simulation. Device performances were most sensitive to the DOS of poly-Si/gate insulator (GI) interface and poly-Si active layer. Deep level states at the poly-Si/GI interfaces strongly affect the subthreshold slope.

1. Introduction

Accompanied with the requirements for high performance poly-Si TFT, many kinds of crystallization technology, including 2 shot SLS (Sequential Lateral Solidification), for high quality poly-Si have been proposed. In the process integration for the poly-Si TFT technology, a comprehensive study on the device characteristics and the relationship among process-, material-parameters and device characteristics are required. Several works based on the device simulation were previously reported[1-3]. To our knowledge, there has been no report on the effect of each DOS parameter on the device characteristics of poly-Si TFT with 2 shot SLS crystallized structure. In this paper, we have investigated the effect of material parameter such as DOS (density of state) of poly-Si and interfaces [poly-Si/gate insulator(GI), buffer layer/poly-Si, and grain boundary (GB)] on threshold voltage (Vth), mobility (µ), and subthreshold slope (S) of 2 shot SLS poly-Si TFT. This work will be useful for the analysis on abnormal characteristics and process optimization for high performance 2 shot SLS poly-Si TFT.

2. Model and device structure for simulation

Two dimensional device simulation was performed by using ATLAS of Silvaco company. Device structure and mesh scheme for this work are shown in Fig. 1(a) and (b), respectively. Channel length (L), width (W), and LDD (lightly doped drain) length are 10 um, 4 um, and 1.5 um, respectively. Mo gate, 1000 Å-thick SiO2 for GI, and 500 Å-thick poly-Si were applied. The N+ poly-Si and LDD have a uniform doping concentration of 1e20 /cm3 and 1e18 /cm3, respectively. In this work, the active poly-Si has primary GBs which are periodically located with the distance of 3.5 um. This distance is typical for 2 shot SLS poly-Si[4]. According to our simulation, the effect of GBs in the highly doped poly-Si (n+ poly-Si) on the electrical characteristics of the TFTs was almost negligible compared with that of GBs in poly-Si and LDD. Therefore, we exclude the existence of GBs in the n+ poly-Si from consideration. Since the GB locations are not uncontrollable, the GBs are randomly located in the active poly-Si region. We assumed that two GBs located at the borders of n+poly-Si/LDD and one GB at the center of the poly-Si, as shown in Fig. 1(a) and (b). Although there are protrusions at the GB positions in the real SLS poly-Si, we also assumed a flat surface of poly-Si layer.

In order to reflect the different structure at the interface such as GBs, poly-Si/GI interface, and buffer layer/poly-Si interface, we used the model of Chou et al[5] in which they defined a very thin poly-Si layer for the interfaces and set different DOS distribution from that of bulk poly-Si region. The dimension of poly-Si regions for the interfaces was assumed as 20 Å-thick and a dense mesh structure was applied for those regions as shown in Fig. 1(b).

Expressions of DOS distributions are given in Eqn (1) and (2). Total density of states (DOS), g(E), is assumed to be composed of four elements; two tail distribution (donor-like and acceptor-like tail distribution) and two deep level bands (one acceptor-like and the other donor-like) which as modeled using a Gaussian distribution.

$$g(E) = g_{TA}(E) + g_{TD}(E) + g_{GA}(E) + g_{GD}(E) \quad (1)$$

$$g_{TA}(E) = NTA\exp\left(\frac{E - E_C}{WTA}\right)$$
$$g_{TD}(E) = NTD\exp\left(\frac{E_V - E}{WTD}\right) \qquad (2)$$
$$g_{GA}(E) = NGA\exp\left[-\left(\frac{E - E_{GA}}{WGA}\right)^2\right]$$
$$g_{GD}(E) = NGD\exp\left[-\left(\frac{E - E_{GD}}{WGD}\right)^2\right]$$

where E is the trap energy and Ec is the conduction band energy, Ev is the valence band energy. $g_{TA}(E)$ and $g_{TD}(E)$ are the tail distribution functions and $g_{GA}(E)$ and $g_{GD}(E)$ are Gaussian distribution functions. The subscripts T, G, A, and D stand for tail, Gaussian (deep level), acceptor, and donor states, respectively. The definitions of DOS parameters are summarized in Table I. Based on Eqn(1) and (2), the DOS distribution of each region is given and an example of the DOS distribution was plotted in Fig. 2.

3. Results

In order to confirm the effectiveness of our device model, we measured the I-V characteristics of a fabricated 2 shot SLS poly-Si TFT and compared the characteristics with a simulated result. As shown in Fig. 3, the simulated result is well fitted to the measured one.

Then, we have investigated the effect of each DOS parameter on the Ids-Vgs characteristics. First, we have obtained an Ids-Vgs curve with reference values of the DOS parameters and then investigated the Ids-Vgs characteristics with the variation of each DOS parameter. The DOS values for the reference TFT are shown in Table. II. In this work, we mainly investigated the effect of DOS parameter related with the acceptor-like traps (NTA, WTA, NGA, and WGA) due to the little effect of the donor-like traps on the N-channel TFT characteristics.

Figure 4(a) shows the Ids-Vgs characteristics of N-channel poly-Si TFTs for the variation of NTA, NGA, WTA, and WGA in the active poly-Si region. As the increases of NTA and NGA, mainly on-current deteriorate. The effect of NGA is more significant than that of NTA. Above NGA>1e18, subthreshold characteristics become worse. As the characteristics decay parameters (WTA and WGA) increase, the subthreshold slope decreases as well as on-current. This trend is similar but more sensitive to the DOS parameters of the poly-Si/GI interface [Fig. 4(c)]. The DOS parameter dependences for the LDD region are shown in Fig. 4(b). In the LDD, an increase of trap state causes the abrupt decrease of the on-current while the subthreshold characteristics near Vgs=0 V remain unchanged even with the wide variation of the DOS parameters.

Figure 4(d) shows the effect of DOS parameters of the GBs. Unlike the results for the poly-Si/GI interface and poly-Si bulk, only NGA affects the TFT characteristics. For example, if the NGA is above 1e19 /cm3, on-characteristics and subthreshold are remarkably degraded. It is thought that a large NGA, corresponding high density of dangling bonds, raises the height of GB barrier against the carrier transport[6] and thereby the transconductance in the channel region was decreased.

The variations of device parameters such as Vth, μ, and S are plotted as a function of DOS parameters in Fig. 5(a)~(l). In order to compare the sensitivity of the device parameter to the variation of DOS parameters in each region, we plotted the results for poly-Si, LDD, poly-Si/GI, buffer/poly-Si, and GB simultaneously in a given graph. From Fig.5(a)~(l), it can be noted that the overall device performance deteriorate with all kinds of DOS parameters. Particularly, the device parameters are very sensitive to the DOS of poly-Si active layer and poly-Si/GI interface. This indicates that the control of the defect density at these two region is most important to improve the TFT characteristics. Meanwhile, there are strong dependences of device parameters on certain DOS parameters. For example, Vth on NGA (≥1e18 /cm3) of GB and buffer/poly-Si interface [Fig. 5(c)], μ on WTA (≥0.05 eV) of LDD, NGA (≥1e18 /cm3) of poly-Si, buffer/poly-Si, LDD, and GB [Fig. 5(f)], and subthreshold slope on NGA (≥5e19 /cm3) of poly-Si/GI interface [Fig. 5(k)].

4. Conclusion

We have investigated the effect of DOS (density-of-state) parameters on the characteristics of a 2 shot SLS poly-Si TFT. It is found that overall device performances are most sensitive to the

DOS of the poly-Si/gate insulator(GI) interface and active poly-Si. Deep level states in TFT strongly affect the mobility and those at the poly-Si/GI interface seriously degrade the subthreshold characteristics as well as the mobility.

5. References

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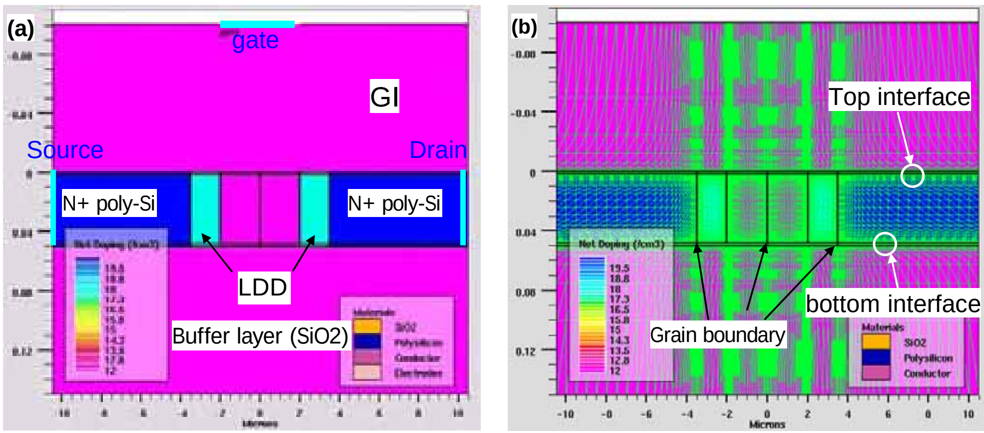

Fig. 1. A device structure for the N-channel TFT simulation (W=10 um, L=4 um, LDD=1.5 um). There are primary grain boundaries at the center of active layer and at the borders of n+ poly-Si and LDD poly-Si regions. In (a), each regions are identified with the doping concentration and materials and a mesh structure for the simulation was shown in (b).

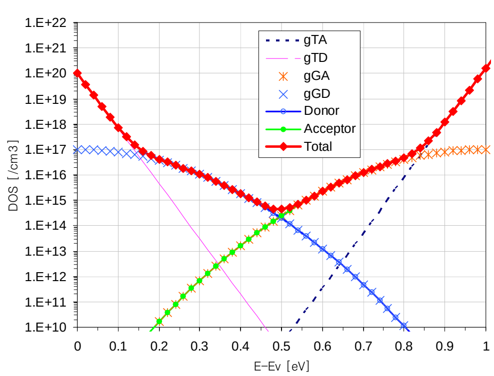

Fig. 2. An example of DOS (Density-of-State) distribution.

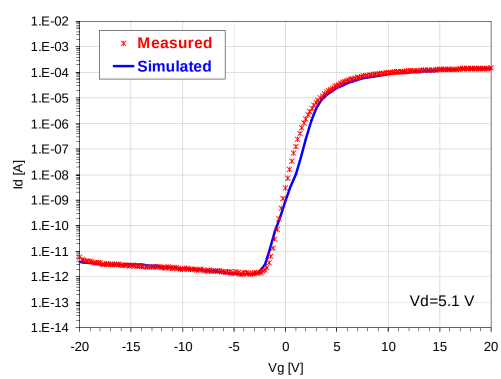

Fig. 3. A fitted result between simulated and measured characteristics. (W/L=10/4, LDD=1.5, Vds=5.1 V)

Table I. DOS parameters and definitions.

Parameter	Definition
NTA	Density of acceptor-like states in the tail distribution at the conduction band edge
NTD	Density of donor-like states in the tail distribution at the valence band edge
WTA	Characteristic decay energy for a tail distribution of acceptor-like states
WTD	Characteristic decay energy for a tail distribution of donor-like states
NGA	Density of acceptor-like states in a Gaussian distribution at the peak position
NGD	Density of donor-like states in a Gaussian distribution at the peak position
EGA	Energy at the Gaussian distribution peak for acceptor-like distribution
EGD	Energy at the Gaussian distribution peak for donor-like distribution
WGA	Characteristic decay energy for a Gaussian distribution of acceptor-like states
WGD	Characteristic decay energy for a Gaussian distribution of donor-like states

Table. II. Values of DOS parameters for the reference TFT.

Region / DOS parameter	Bulk DOS			Interface DOS		
	S/D	LDD	Active	Poly-Si/GI	Buffer/poly-Si	Grain boundary
NTA	1e21	1e20	1e19	1e20	1e19	1e19
NTD	1e21	1e20	1e19	1e20	1e19	1e19
WTA	0.01	0.01	0.01	0.01	0.01	0.01
WTD	0.01	0.01	0.01	0.01	0.01	0.01
NGA	1e18	1e18	1e18	1e19	1e18	1e18
NGD	1e18	1e18	1e18	1e19	1e18	1e18
EGA	0	0	0	0.4	0.4	0.4
EGD	0	0	0	0.4	0.4	0.4
WGA	0.1	0.1	0.1	0.1	0.1	0.1
WGD	0.1	0.1	0.1	0.1	0.1	0.1

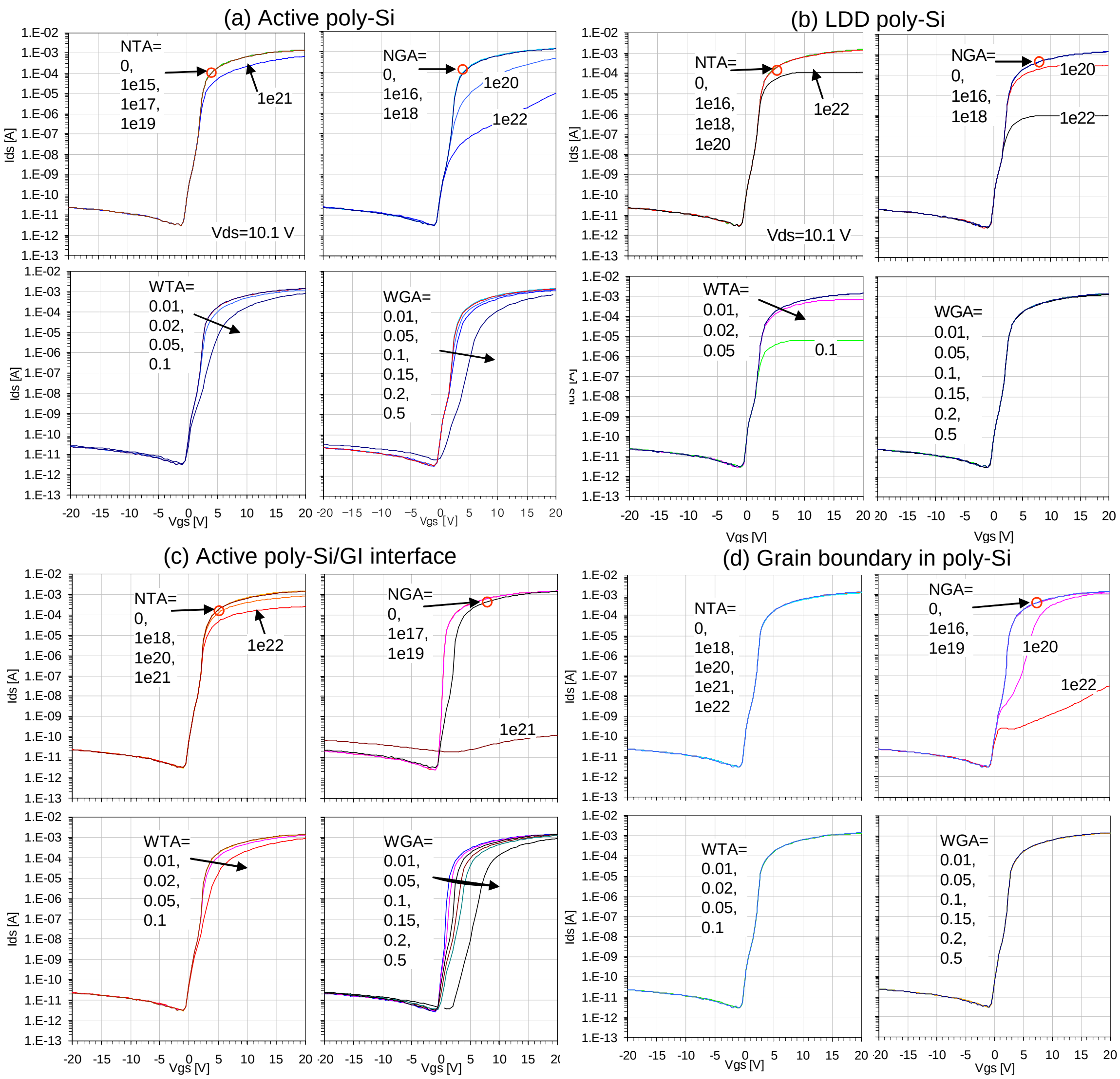

Fig. 4. Ids-Vgs characteristics for the variation of DOS parameters (NTA, NGA, WTA, and WGA) in each region (Vds=10.1 V): (a) Active layer (poly-Si) (b) LDD (c) Active/GI(gate insulator) interface and (d) Primary grain boundaries(GBs).

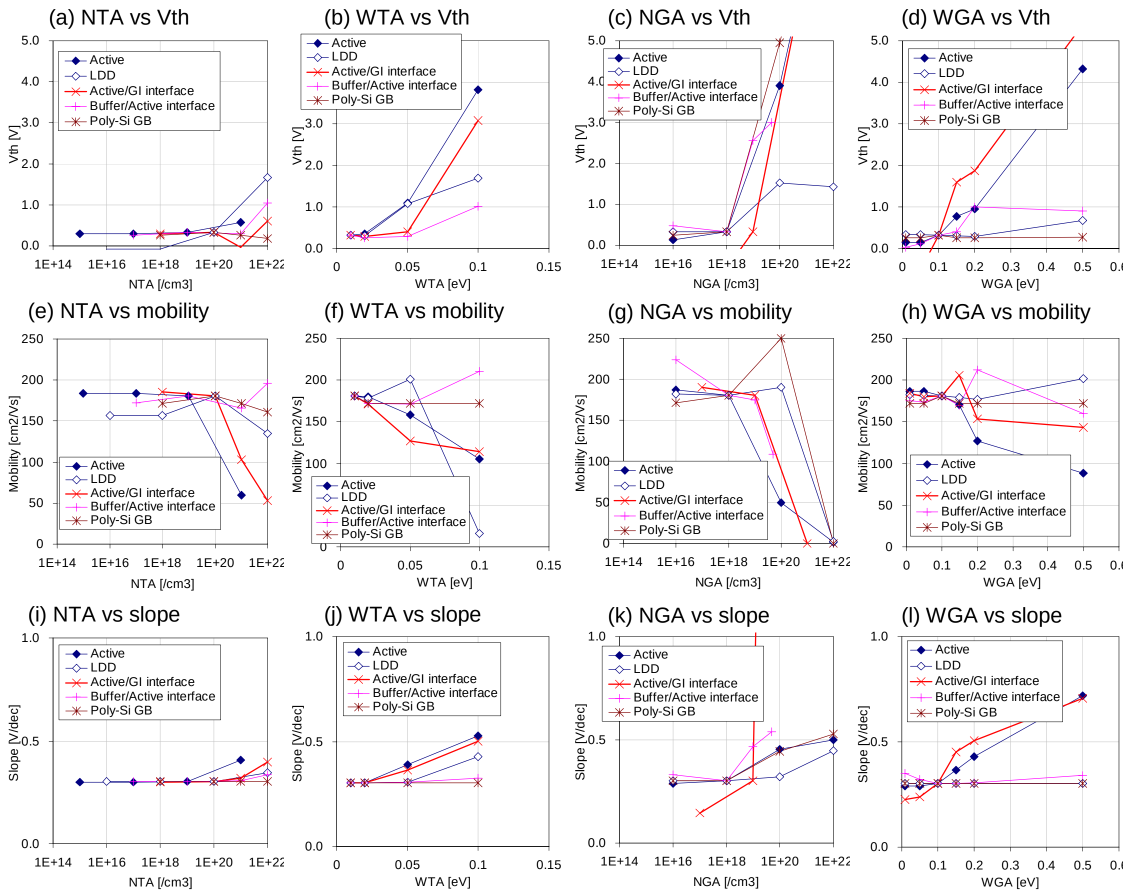

Fig. 5. Device parameters (Vth, mobility, and slope) as a function of DOS parameters (NTA, NGA, WTA, and WGA) in each region. The device parameters were extracted from the Ids-Vgs characteristics in Fig. 4.