Importance of Gate SiN_x Properties Related to a-Si:H TFT Instability

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Abstract

Properties of silicon nitride (SiN_x) film including physical and electrical characteristics have been studied for improving the stability of hydrogenated amorphous silicon thin-film transistors (a-Si TFTs) in active-matrix liquid-crystal displays (AMLCDs). The instability of a-Si:H TFTs is estimated by accelerated stress test of both bias-temperature stress and bias-illumination stress. The results show that the deposition conditions of SiN_x films with higher power and lower pressure are the best choice for improving the on-current and stability of TFTs.

1. Introduction

Hydrogenated amorphous silicon TFTs (a-Si:H TFTs) with SiN_x gate insulator are widely used as switching devices in active-matrix liquid-crystal display (AMLCD). In TFT-LCD displays, it is important to ensure that the reliability of TFTs should be stable enough to assure the quality of displays. The deterioration of on-current (I_{on}), off-current (I_{off}), and threshold voltage (V_{th}) is a considerable evidence to determine the reliability performance of TFTs [1,2]. The a-Si:H TFTs exhibit threshold voltage shifts after prolonged bias to gate electrode. Charge trapping in the gate dielectric and defect-state creation in the a-Si:H are two main mechanisms to explain the electrical instabilities [3,4]. Moreover, a defect-pool model has been proposed by Powell's early work to clarify the important influence of the state creation on degrading the electrical characteristics of a-Si:H TFTs [4]. The a-Si:H TFTs in LCD are practically used under backlight and lighting environment. It is important to estimate the stability of a-Si:H TFTs under light illumination. In this report, we investigate the instability of a-Si:H TFTs not only by accelerated stress of DC bias voltage and temperature but also by long-term stress of DC bias voltage under light illumination. The effect of gate SiN_x properties and a-Si:H/SiN_x interface on the instability of a-Si:H TFTs is studied. It is observed that a fine-tuning process is necessary to get better deposition uniformity and reliability performance of SiN_x film as the gate insulator of TFTs.

2. Experimental

The fabrication process of a-Si:H TFTs used in the bias stress experiment was similar to that of a conventional inverted-staggered bottom-gate back-channel-etched (BCE) a-Si:H TFT. In this work, a-Si:H TFTs with different deposition conditions of gate SiN_x films, especially the process parameters of pressure and power, were fabricated to examine the effect of gate SiN_x properties and a-Si:H/SiN_x interface on the instability induced by a gate bias stress. Three TFT samples with SiN_x films deposited at different conditions were called as sample A, B, and C, respectively, as listed in Table 1. The SiN_x films as the gate dielectrics of sample A, B, and C were deposited at low power with high pressure, high power with high pressure, and high power with low pressure, respectively. All samples were annealed at 200°C for 2 hours and cooled before each bias stress measurement to restore the initial TFT transfer characteristics (I_{ds}-V_{gs}). There were two kinds of measurements in this work to investigate the instability of TFTs with different gate-insulator SiN_x.

Table 1. The deposition conditions of SiN_x films as gate dielectrics of TFT sample A, B, and C.

Sample	deposition conditions of SiNx	
	RF power	Pressure
A	low	high
B	high	high
C	high	low

2.1 TFT instability characteristics

The initial I_{ds}-V_{gs} curves of TFTs were measured at 80°C, then TFTs were supplied with a gate bias of 30 V for 2 hours where drain and source terminals were grounded. After the stress was accomplished, I_{ds}-V_{gs} curves of TFTs were measured again to compare the characteristics degradation of TFTs. Another measurement condition was done under backlight illumination of 2500 nits with the same gate bias stress to simulate a real panel operation with backlight.

2.2 Gate SiN_x breakdown characteristics

The measurement condition for gate SiN_x breakdown characteristics was that the bias voltage of electrodes swept from 0 to 500 V and its ramped rate was 0.12 $MVcm^{-1}s^{-1}$. We recorded the current of the gate and plotted the current as a function of voltage. The capacitor test-key with MIM structure was analyzed to investigate the breakdown characteristics of SiN_x films deposited at different deposition conditions.

3. Results and Discussion

3.1 TFT instability characteristics

Figure 1 shows the transfer characteristics (I_{ds}-V_{gs} curves) of a-Si:H TFTs before and after bias stress. I_{on}, V_{th}, and I_{off} parameters of a-Si:H TFTs are extracted from I_{ds}-V_{gs} curves for further analysis.

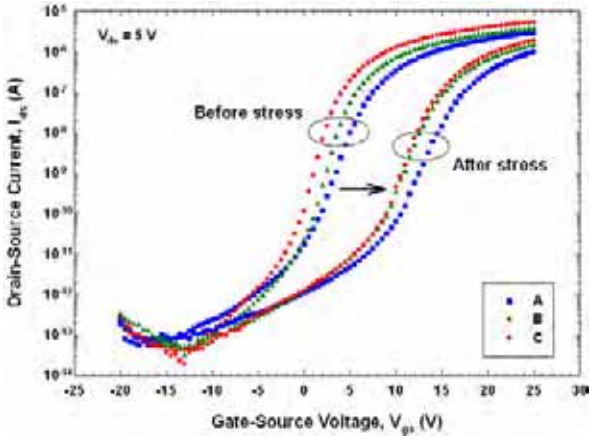

Figure 1. Transfer characteristics (I_{ds}-V_{gs}) of sample A, B, and C at V_{ds} = 5V. Curves labeled "Before stress" are measured before stress and curves labeled "After stress" are measured after bias-temperature stress with V_{gs} = 30V at 80°C for 2 hours.

Firstly, I_{on} is degraded with increasing stress time as shown in Fig. 2(a). Sample A is the worse case with lower I_{on}. The I_{on} of Sample B is larger than that of sample A initially but is degraded faster after stressing. Sample C with higher quality SiN_x gate insulator can get higher I_{on} even after stressing for 24 hours and I_{on} degradation rate is also slow. The degradation of TFT electrical performance is due to the state creation in the interface between a-Si:H and gate SiN_x [5]. Besides, V_{th} and I_{off} are the important TFT electrical properties to judge device performance [6]. From Figure 2(b), the shift of V_{th} is lower for sample C. I_{off} is kept at the same level for all samples as shown in Fig. 2(c).

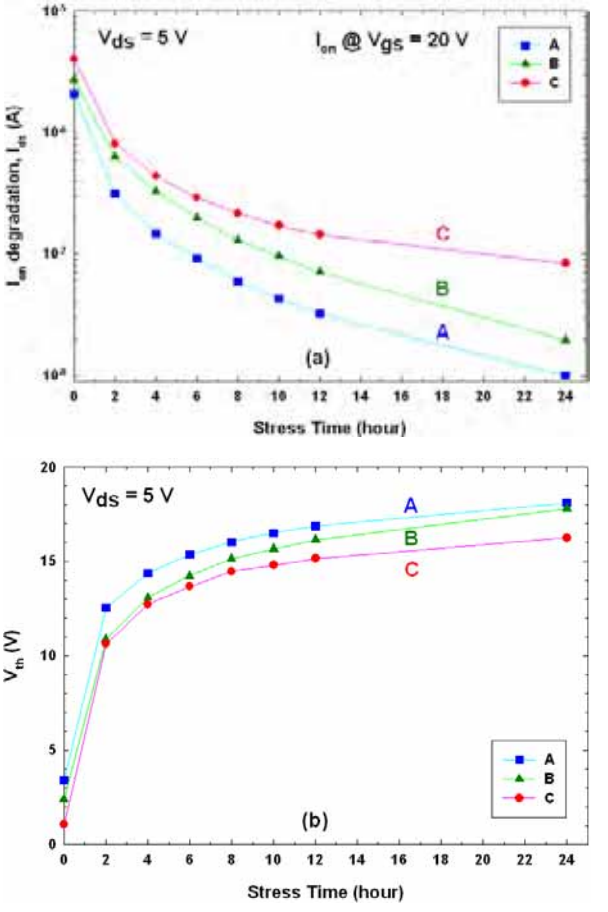

Figure 2. (a) on-current (I_{on}) degradation and (b) threshold voltage shift (V_{th}) distribution of sample A, B, and C under bias-temperature stress as a function of stress time. I_{on} is measured at V_{gs} = 20V.

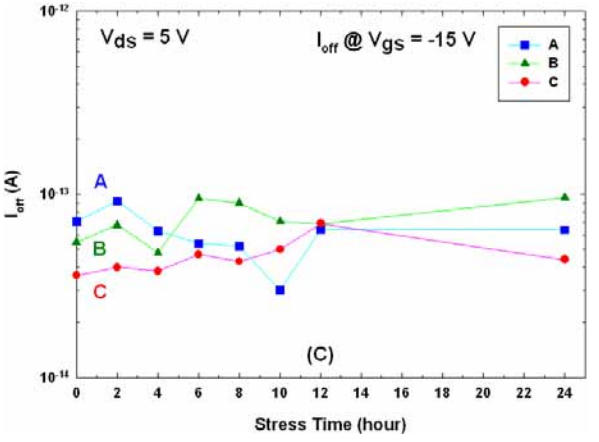

Figure 2. (c) off-current (I_{off}) distribution of sample A, B, and C under bias-temperature stress as a function of stress time. I_{off} is measured at V_{gs} = -15V.

To simulate the panel operation, we investigate TFT instability under light illumination. The I_{on}, V_{th}, and I_{off} characteristics of TFTs samples as a function of stress time are shown in Fig. 3(a), (b), and (c), respectively. Compared with the results of bias-temperature stress, sample C still possesses a lower I_{on} degradation, less V_{th} shift, and lower I_{off} after stressing. In addition, the I_{on} degradation of TFT samples under bias-illumination stress is slower with increasing stress time as compared with that of TFT samples are stressed under dark environment at 80°C. It indicates that the deterioration of TFTs resulting from the bias-temperature stress with high temperature of is considerably rapider than that of TFTs arising from bias-illumination stress.

It is known that the state creation is the dominant mechanism up until a critical gate voltage but charge trapping becomes significant thereafter [3]. The critical voltage at which charge trapping overtakes state creation is dependent on the bandgap and quality of SiN_x film, which also confirmed that the charge trapping process is nitride related.

The sample C of TFT with a denser SiN_x as the gate insulator possesses a lower density of trapping centers within the SiN_x film. Therefore, the state creation in the a-Si:H layer or at the a-Si:H/SiNx interface and charge trapping in the nitride layer of sample C with a quality-improved SiN_x as the gate insulator have been reduced during both bias-temperature stress and bias-illumination stress.

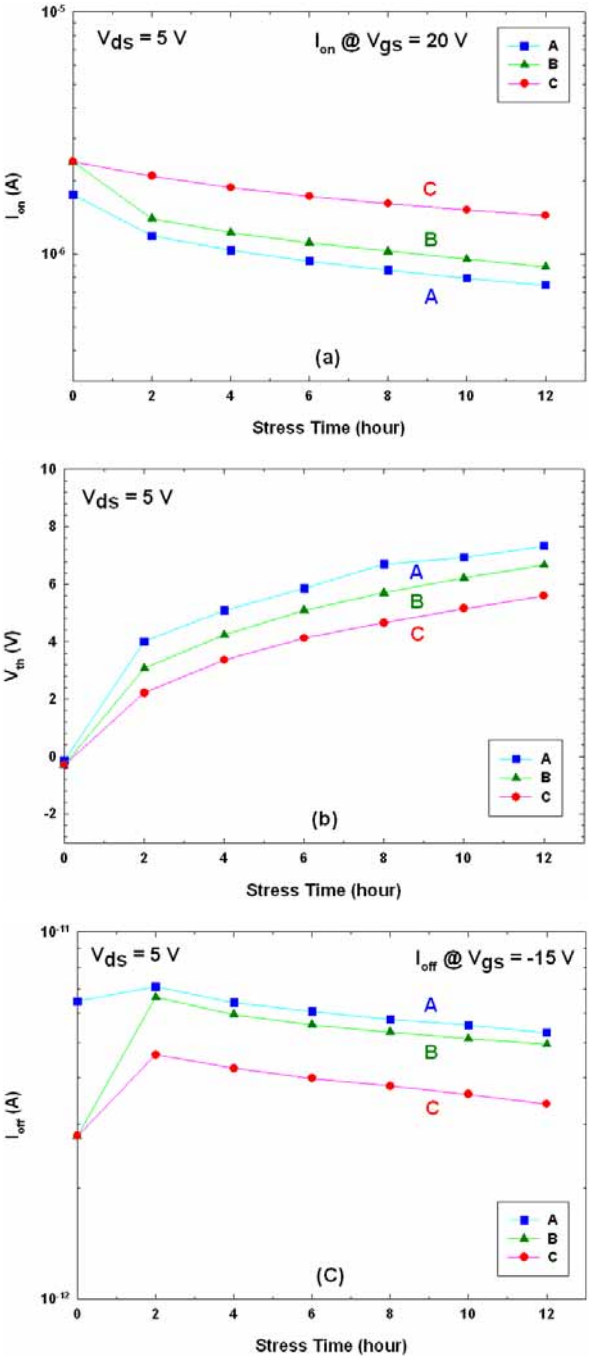

Figure 3. (a) on-current (I_{on}) degradation, (b) threshold voltage shift (V_{th}), and (c) off-current (I_{off}) distribution of sample A, B, and C under bias-illumination stress as a function of stress time. I_{on} is measured at V_{gs} = 20V and I_{off} is measured at V_{gs} = -15V.

3.2 Gate SiN_x breakdown characteristics

Breakdown behavior of SiN_x film has been well known and is widely discussed in semiconductor applications [7]. The quality of SiN_x film can be improved continuously even though gate SiN_x film becomes thinner and thinner for cost down in panel manufacturer. We use the following methodology to define the dielectric breakdown voltage from I-V curves of capacitors with MIM structure. When the bias voltage reached the critical voltage, which is defined as the dielectric breakdown voltage, there is an immediate steep rise of current in the multiple of 10. Figure 4 shows the breakdown electric field of SiN_x films as the gate insulator of TFT sample A, B, and C. The breakdown voltage of all samples is high enough to work steadily in a real panel operation.

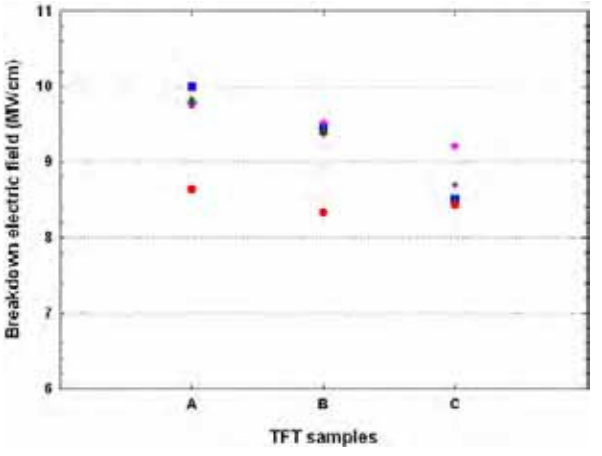

Figure 4. Breakdown electric field of SiN_x films as gate insulators of sample A, B, and C at different locations.

However, the SiN_x film as the gate insulator of sample C possesses a slightly lower breakdown filed but has a better uniformity.

4. Conclusions

Gate SiN_x film with different properties has a fatal effect upon the instability and reliability of a-Si:H TFTs. The deposition condition for gate SiN_x film has been optimized to get good TFT stability and SiN_x film reliability. In this condition state creation has been reduced during bias-temperature stress and bias-illumination stress. Therefore, although many process issues are critical to the TFT performance, the optimized modifications in CVD process for the SiN_x gate dielectric deposition should be taken into consideration in preparing the high performance a-Si:H TFTs.

5. References

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