Transparent ZnO Thin Film Transistor Array by Means of Plasma Enhanced Atomic Layer Deposition

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Abstract

We have developed ZnO TFT array using conventional photolithography and wet etching processes. Transparent 20 nm of ultra thin ZnO film deposited by means of plasma enhanced atomic layer deposition at 100°C was used for the active channel. The ZnO TFT has a mobility of 0.59 cm^2/V.s, a threshold voltage of 7.2V, sub-threshold swing of 0.64V/dec., and an on/off ratio of 10^8.

1. Introduction

Transparent electronics has attracted many interests, for it can open new applications for consumer electronics, transportation, business, and military.[1] Among them, display backplane, thin film transistor (TFT) would be the most attractive application. The TFTs used for the display are usually classified by their channel materials. In the case of silicon, there are three different kinds of TFTs such as a-Si, microcrystalline Si, and poly Si TFT according to the silicon phase. These TFTs have been intensively investigated. However, they still need improvement for the OLED driving. In addition, these are not good candidates when we want to achieve transparency. Although organic TFTs have been studied as display backplanes, their poor performance led us explore new channel materials.

Many researchers have been investigating oxide semiconductors for transparent channel material of TFT.[2,3] Among them, wurtzite structured wide band gap ZnO thin films have been studied as an active layer in the thin film transistor (TFT) because of their low cost, low photo sensitivity, no environmental concerns, and especially moderate mobility.[4,5] In addition, low temperature process of ZnO opens new way to the flexible display backplane.

Recently we have fabricated 2.15 inch transparent AM-OLED panel composed of 176 x 144 (106 dpi) transparent pixels driven by ALD grown ZnO-TFT.[6] Although we could develop ZnO process having reasonable TFT characteristics by ALD, the ALD grown ZnO-TFT showed sensitivity according to the wet patterning process and operated in a depletion mode with high sub-threshold swing. These are associated with the interface between ZnO and the gate insulator, and we wanted to investigate the effect of ZnO process on the TFT characteristics.

In the present work, we studied the device characteristics of ZnO TFT deposited by means of plasma enhanced atomic layer deposition (PEALD). In PEALD method, plasma-induced damage to a gate insulator layer could be minimized to result in well behaved TFT property, for PEALD uses pulsed plasma with a short pulse time.

2. Experimental

For the film analysis, ZnO films were deposited on the alumina coated p-type Si(100) substrates by means of PEALD at the substrate temperature of 100°C using diethylzinc (DEZ) as Zn precursor and oxygen plasma as oxygen precursor in shower head typed reactor (Genitech MP-1000). The reactor pressure was 3 Torr. One PEALD cycle for the ZnO film growth consisted of the sequential injection of DEZ (4 seconds), Ar (4.5 seconds), O_2 gas (60 sccm, 1.0 seconds), and Ar (0.5 seconds). Radio frequency (RF) pulse was applied during the injection of O_2 gas for 1.0 seconds with RF power of 60W. The flow rate of a purge Ar gas was 80 sccm during the deposition.

The crystallographic orientation of the ZnO films was determined by an x-ray diffractometer (XRD) with CuKα radiation.

For the fabrication of TFT array, 130 nm thick ITO coated glass was used for the substrate. After patterning of ITO (gate) by lithography, alumina was deposited with the thickness of 170 nm at the temperature of 250°C by means of ALD, followed by gate metal pad opening by wet etching of alumina. ALD-deposited Al doped ZnO (ZnO:Al) was used as a source and a drain electrodes and patterned by wet precess. The ZnO semiconductor films were deposited by means of PEALD as described above with 100 cycles and patterned using diluted acid. Fig. 1 illustrates the cross sectional view of unit TFT and optical image of TTFT array.

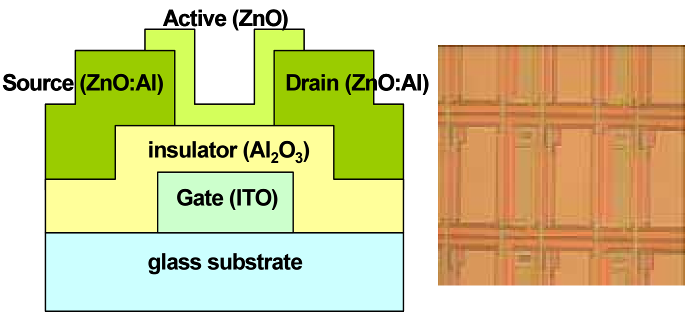

Figure 1. The structure of TFT and optical image of pixels in the array.

3. Results and Discussion

The growth rate of ZnO film at 100°C was 2.0 Å/cycle. Fig. 2 shows the AFM and SEM image. The ZnO thin film grown on a alumina at 100°C shows very flat morphology with RMS value of 2.37Å.

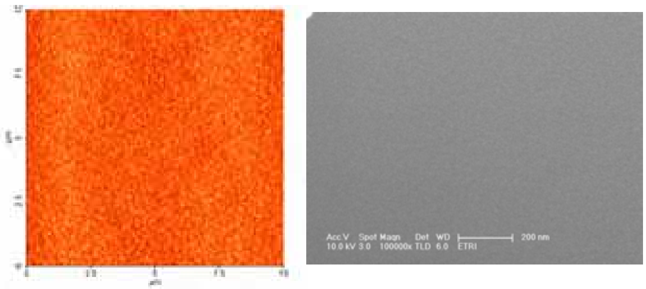

Figure 2. AFM and SEM images of ZnO film grown on the alumina gate insulator

X-ray diffraction patterns of ZnO grown by 100 repeated cycles showed more or less a random orientation with (100) and (002) directions as shown in Fig. 3. The ZnO films with (002) orientation have been usually observed for the films grown by various fabrication methods because the c-plane is the most densely packed plane in the wurtzite structure. In our system, however, the ZnO grown with oxygen plasma at 100°C had mostly (100) orientation as shown in Fig. 3.

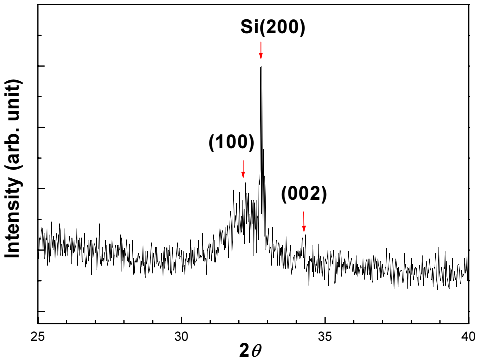

Figure 3. XRD patterns of ZnO films deposited on alumina gate insulator by PEALD

The device with ZnO grown with the lowest plasma power of our system at 100°C showed well behaved TFT characteristic. Fig. 4 shows transfer characteristics of ZnO-TFT for V$_{DS}$ varying from 1 to 21V.

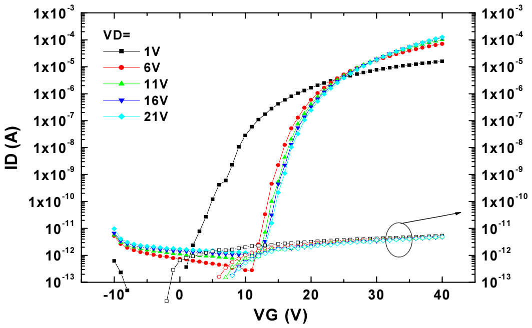

Figure 4. Transfer characteristics of ZnO-TFT with a W/L=100/10 for V$_{DS}$ varying from 1 to 21V.

One of the great advantages of PEALD method for growing ZnO is the decrease of the carrier density in the film by reducing oxygen vacancy due to the reactive oxygen precursor. Compared to that by ALD, PEALD grown film is too dielectric to measure carrier density by Hall measurement system. This can be confirmed from the transfer characteristics of ZnO TFT. The off current is less than 10^{-12}A and lower by 10^{-2} than that of ALD grown TFT. The on/off current ratio is about 10^8. One very unique property is that first measurement of device (measuring at 1V) induced kinds of charge accumulation thus the transfer characteristics were quite different from those measured second time (@ 6 V) or third time (@ 11 V) and so on.

The PEALD grown ZnO TFT exhibit normally-off characteristics with the field effect mobility of about 0.59 cm^2/V.s and threshold voltage of 7.2V. The sub-threshold swing, S.S., is 0.64V/dec. The field effect mobility of PEALD grown ZnO-TFT is rather lower than that of ALD-grown one. We suspect that it may be due to the too low carrier density of ZnO film. The S.S. value is decreased compared to that of ALD grown TFT.

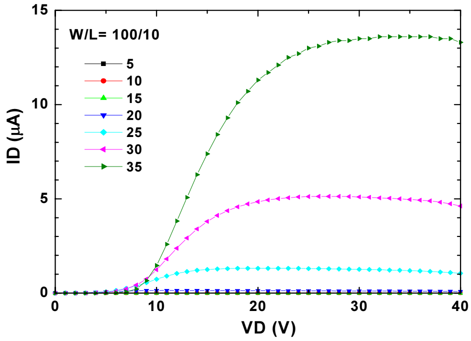

Figure 5. Output characteristics for a ZnO-TFT with a W/L=100/10 for V_{GS} varying from 5 to 35V.

Fig. 5 depicts a set of drain current-drain voltage curves for each gate voltage between 5 and 35V. We easily notice the contact resistance between the S/D and active layer. It might be due to the surface oxidization of ZnO:Al electrode during the ZnO process. The increased threshold voltage also indicates that the plasma process of active layer caused some damage to dielectric layer. The process optimization is under investigation.

To prove the effect of active layer process to the S/D and dielectric layer, we adapted bi-active layer consisting of ALD-grown ZnO as the first layer and PEALD grown ZnO as the second layer. Fig. 6 shows a set of [log (I_D)-V_{GS}] transfer curves with V_{DS} ranging from 1V to 21V and gate leakage current [log (I_G)-V_{GS}] and output characteristics for bi-active layer ZnO-TFT. Fig. 6 depicts drain current-drain voltage curves with clear current saturation for each gate voltage between -5 and 25V. We can easily see the good ohmic contact for the source/drain region to active region. ALD grown ZnO layer acted as the buffer layer to prevent the oxidation of S/D electrode.

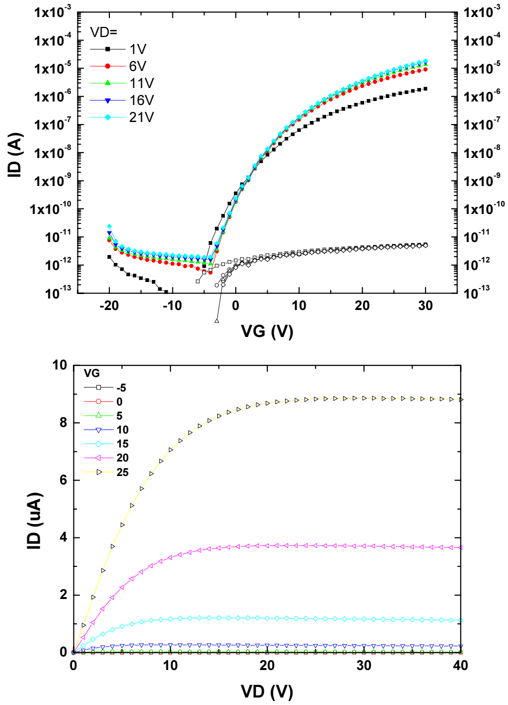

Figure 6. Transfer characteristics and output characteristics for a bi-active ZnO-TFT with a W/L-100/10.

To check the device reliability, we investigated the hysterisis of as fabricated device. Fig. 7 shows the hysterisis loop of ZnO TFT swept from 0 V to 30 V. The counter clockwise hysterisis loops show the biggest memory window of about 2.7 V.

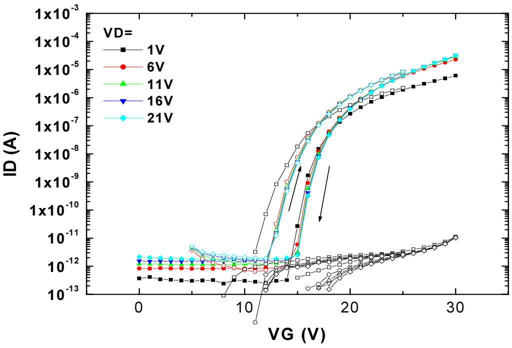

Figure 7. Hysterisis loop of ZnO-TFT for V_{DS} varying from 1 to 21V.

One thing noticeable is the environmental stability of PEALD grown ZnO-TFT. It is well know that surface gas chemisorption of ZnO induce TFT degradation thus, require proper passivation of TFT.[7] However, PEALD grown ZnO film showed quite stable behavior and the TFT characteristics was not changed after 3 weeks standing in the atmosphere.
The inert characteristics of PEALD grown ZnO film could allow us to use various passivation technology.

4. Conclusion

We fabricated transparent ZnO-TFT array by means of PEALD using conventional lithography and wet etching process for the first time. Although the characteristics of PEALD grown ZnO-TFT is not good compared to that of ALD grown TFT in terms of mobility and V_{th}, the S.S. value is reduced and the environmental stability is increased even after wet etching process. The interface modification and S/D electrode change could improve the TFT characteristics.

5. Acknowledgements

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6. References

[1] H. Ohta and H. Hosono, Materialtoday, (2004) 42.

[2] J. Wager, Science, 300 (2003) 1245.

[3] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hiranoo, and H. Hosono, Nature, 432 (2004) 488.

[4] E. M. C. Fortunato, P. M. C. Barquinha, A. C. M. B. G. Pimentel, A. M. F. Goncaives, A. J. S. Marques, R. F. P. Martins and L. M. N. Pereira, App. Phys. Lett., 85 (2004) 2541.

[5] Y. Kwon, Y. Li, Y. W. Heo, M. Jones, P. H. Holloway, D. P. Norton, Z. V. Park, and S. Li, App. Phys. Lett., 84 (2004) 2685.

[6] Sang-Hee Ko Park, Chi-Sun Hwang, Jeong-Ik Lee, Sung Mook Chung, Yong Suk Yang, Lee-Mi Do, and Hye Yong Chu, Proceeding of SID 06, (2006) 25.

[7] David Honga and John F. Wager, J. Vac. Sci. Technol. B 23 (2005) L25.