Forming Low-Resistivity Electrodes of Thin Film Transistors with Selective Electroless Plating Process

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Abstract

The silver gate and source/drain electrodes for an a-Si thin film transistor were fabricated by the selective electroless plating (SELP) process. Relevant physical properties including taper angle, uniformity and resistivity are investigated. The Ag layer was about 150nm to 250nm thick, the resistivity less than $3x10^{-6}$ Ohm-cm and the taper angle 45° - 60° and the nonuniformity less than 10% on G2 substrates. The transfer characteristics with the Ag gate, and source/drain electrodes respectively possessed good field effect mobility similar to conventionally fabricated a-Si TFTs. This process provided low resistivity, low cost and ease of processing.

1. Introduction

As the panel size increases and the resolution requirements become higher, the problem of RC delay in the metal lines of the panel becomes more important. At the moment, the risks due to high metal line resistance will appear in the next generation TFT LCD manufacturing. Simplified processing steps are important considerations also. We have investigated the fabrication processes using Ag thin films as the gate and source and drain electrodes for the a-Si TFTs which can provide lower line resistance than Al and Cu.

Electroless plating process is a conventional process which has been widely used in the printed circuit board (PCB) industry today. Such wet processes possess many advantages, such as low cost and lower process temperature etc. Although the film uniformity control and the bath parameters control are important issues to be resolved. This paper will discuss the SELP fabrication process for the deposition of the gate or the source and drain Ag electrodes in an a-Si TFT. The film characteristics and the TFT electrical characteristics for a-Si TFTs with the Ag gate or Ag source and drain electrodes will be presented.

2. Results

Figure 1 illustrates the cross sectional view of the a-Si TFT, which was the inverted staggered structure. A non-alkaline glass was used as a substrate. After patterning of photoresist by lithography, Silver was deposited at the temperature of 60 ℃ by means of electroless plating process. The gate pattern was formed after the stripping of the photoresist. The SELP process, combined with a lift-off process is used to pattern the electrode without the etching process. Figure 2 illustrates the process flow. (1) The substrate is first covered with a 1 μ m thick photoresist by spin coating and the photolithography is used to produce negative patterns in the photoresist. (2) A seeding layer is applied with coating process. (3) The pattern is formed by removing the photoresist. (4) The electrodes, around 230nm thin layer of silver is deposited on the remaining seeding area. The resistivity of electrode film is about $3x10^{-6}\Omega$-㎝ and the resultant taper angle of gate electrode is 45° in the figure 3. with the isotropic desposition. The nonuniformity of the electrode film is 7.82% with the average 230nm thickness on G2 substrate shown in the figure 4.

After the patterning of the Ag gate electrode, the tri-layer, SiNx, a-Si：H, and n^+ a-Si：H layers were deposited by using in-situ PECVD method at temperature 200 ℃ . After the process, the photolithography process was used to define the channel of the TFT device. The source and drain electrode was deposited by using sputter method and the material we used was MoW. The electric characteristic of TFT device was measured by HP-4145 Semiconductor parameter analyzer. Figure 5 (a) and (b) shows the transfer (log I_D-V_G) and output (I_D-V_{DS}) characteristic of the TFT device with Ag gate electrode, respectively. The channel width and length of the device is 100 and 10 μm respectively. From

Figure 4 (a), the on current was about 9 μA at V_D = 10 V and V_G = 20 V. The leakage current was also observed to be about 5 pA at V_D = 10 V and V_G = 0 V. Therefore, on/off current ratio of 1.8×10^6 was obtained. The electron field effect mobility at saturation is 0.1 $cm^2/V \cdot sec$, and the threshold voltage is 4.1 V.

Separately the source and drain electrodes of the TFT were replaced with thin film Ag layer which was deposited by electroless plating process. Figure 6 (a) and (b) shows the transfer characteristic of the a-Si TFT device with the Ag source and drain electrodes. The channel width and length are the same as mentioned above. From the transfer characteristic of the device, the I_{ON} was measured about 8 μA at V_D = 10 V and V_G = 20 V. The leakage current was also measured about 10^{-11} A at V_D = 10 V and V_G = 0 V in the same figure. The on/off ratio is about 1×10^6, and the threshold voltage is 2.34 V.

3. Conclusion

The study has shown the feasibility for the replacements of the electrodes of TFT with silver by using electroless plating method. SELP technique not only can avoid expensive, time-consuming process steps but also can be combined with conventional processes. Although there are still some challenges in the further development of the SELP technique, its simplicity makes it a very favorable technique to integrate Ag-based TFT to the large area panel.

4. Acknowledgements

The authors would like to thank Dr. Fan Luo, CTO of AU Optronics Corp., for many useful discussions. This work was supported by the Taiwan TFT-LCD Association (TTLA) under Contract No. A623TT1000.

5. References

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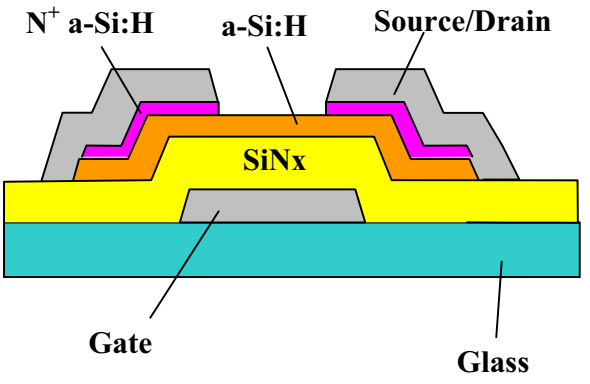

Figure 1 Cross sectional view of the TFT

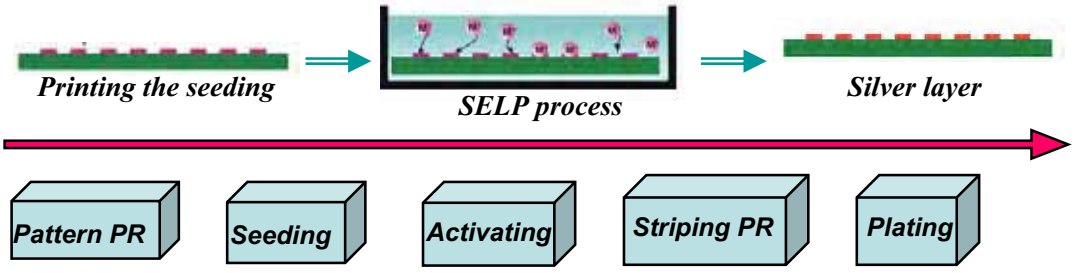

Figure 2 SELP and Lift-Off processes

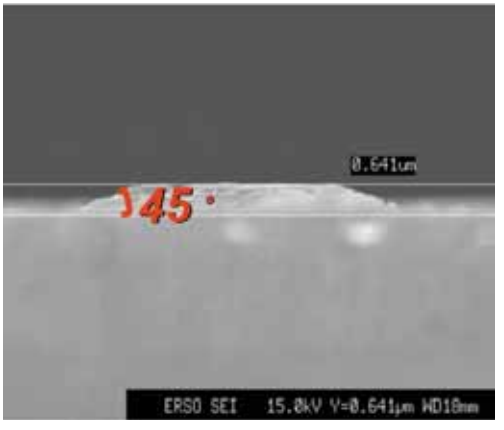

Figure 3 The taper profile of silver gate electrode

Figure 4 The average 230nm thickness with 7.82% uniformity on G2 substrate

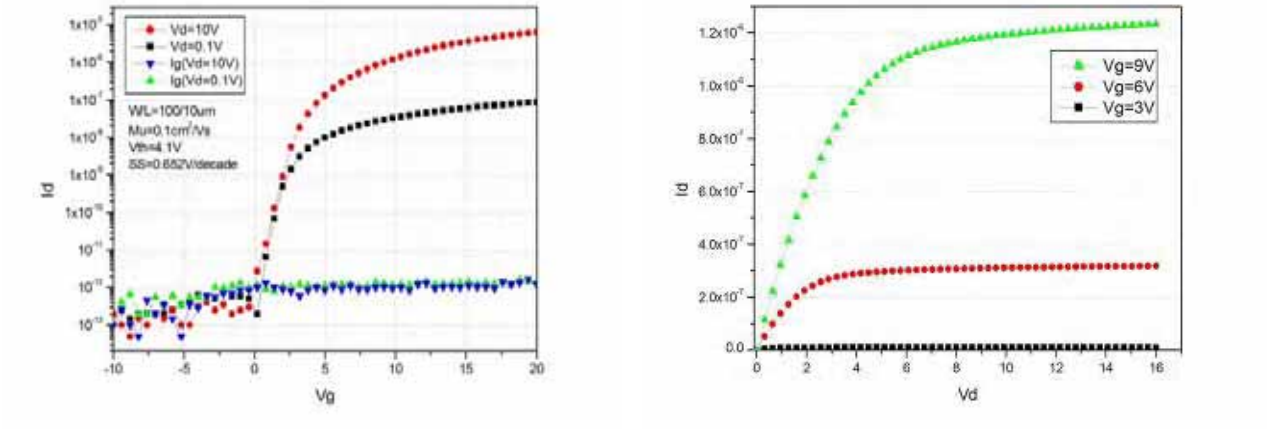

Figure 5 The I-V curve of the TFT with silver gate electrode
（a）I_d-V_g (b) I_d-V_d

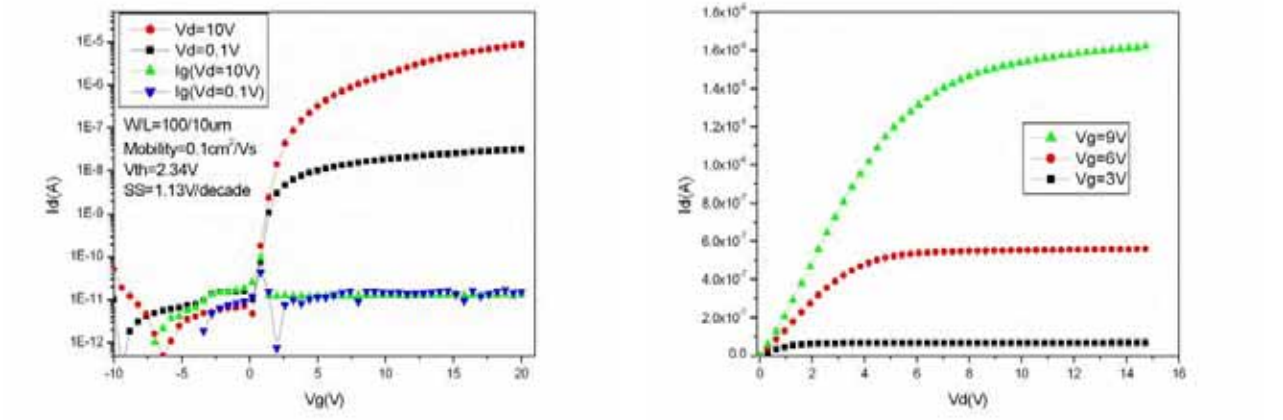

Figure 6 The I-V curve of the TFT with silver source/drain electrode
（a）I_d-V_g (b) I_d-V_d