Development of Rapid Thermal Processor for Large Glass LTPS Production

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Abstract

VIATRON TECHNOLOGIES has developed Field-Enhanced Rapid Thermal Processor (FE-RTP) system that enables LTPS LCD and AMOLED manufacturers to produce poly-Si films at low cost, high throughput, and high yield. The FE-RTP allows the diverse process options including crystallization, thermal oxidation of gate oxides and fast pre-compactions. The process and equipment compatibility with a-Si TFT lines is able to provide a viable solution to produce poly-Si TFTs using a-Si TFT lines.

1. Introduction

Production cost of flat panel displays becomes increasingly important, as their prices are going down. For AMOLEDs and LTPS LCDs to compete in the display markets, their production costs also should be lowered. Since those displays use the poly-Si TFT backplane, low cost production of the poly-Si panel is important. The best scenario to achieve this is to produce poly-Si TFT backplane in the existing a-Si TFT lines. The use of a-Si TFT lines will be particularly beneficial for AMOLED, since it will compete with a-Si TFT LCDs cost-wise in the middle and large display products in near future. To realize the production of poly-Si in a-Si lines, following prerequisites should be met; capability of processing large glass substrate, process compatibility with a-Si TFTs, and availability of process tools of large glass substrates.

Recently, the field enhanced rapid thermal processor (FE-RTP), which enables production of poly-Si, is commercially available. The system can process up to Gen. 4 glass, and will process Gen. 5 glass in this year. Many display makers have successfully demonstrated AMOLEDs and LTPS LCDs using FE-RTP [1-3].

The most important feature of FE-RTP is high temperature process capability up to 800°C without glass damages. This allows TFT manufacturers to expand their available process options. This paper reviews some of those process options including solid phase crystallization of a-Si, thermal oxidation of gate oxide, and pre-compaction of glasses.

2. Results

FE-RTP system.

Fig. 1. Layout of FE-RTP system

The precept of FE-RTP system is uniform heating and cooling of glass substrates in a combination with rapid heating function. Schematic description of FE-RTA system is shown in Fig. 1. The system is of an in-line design consisting of multiple temperature control modules (TCM) and an FE-RTP process module (PM). The TCMs sequentially heat and cool the glasses. Uniform heating and cooling of glass substrate is found to be essential in preventing glass damage and attaining uniform poly-Si. The TCM with multi-zone temperature controls provides temperature uniformities of glasses within ±2°C.

The PM located between heating and cooling modules enhances the crystallization kinetics thus accelerating the process. The FE-RTP heat treatment involves rapid thermal heating of glass in combination with alternating magnetic field induction to enhance the heating efficiency [4].

Fig. 2 shows the glass flatness after FE-RTP heat treatments at various temperatures. Their values are compared with normal glass without heat

treatments. The FE-RTP can produce a glass without any glass warpage up to the temperature of ~800°C.

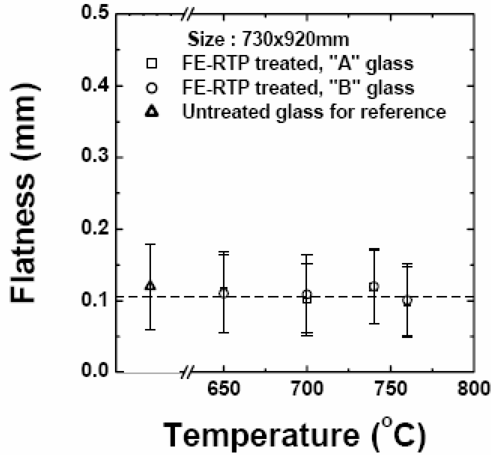

Fig. 2. Flatness of Gen. 4 glasses after FE-RTP processes as a function of pre-heating temperatures.

Crystallization

The FE-RTP enables the manufacturers to produce poly-Si with the quality specific to target applications. Fig.2 shows the TFT mobilities for various non-laser crystallization methods using FE-RTP system. The solid phase crystallization (SPC) is the simplest process. Typical mobility values of SPC poly-Si are 20~50 cm^{2}/V.sec.

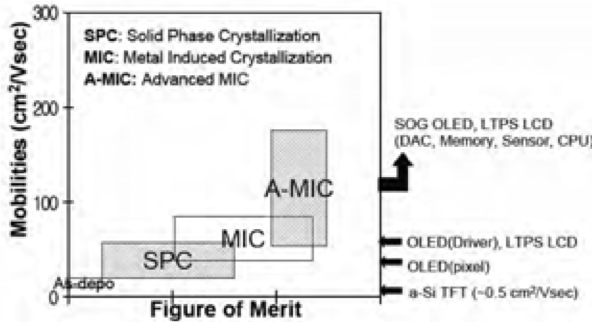

Fig. 3. Typical mobility ranges for various crystallization methods using FE-RTP

The mobility is high enough for pixel operation as well as some driver integration. Key advantage of SPC process is the uniformity. SPC poly-Si has a number of defects in grains. The defects have been considered to be detrimental to TFT performance, and efforts have been made to reduce the intra-granular defects. However, we believe that those defects plays important role in the uniformity via. reduction of grain size effects. Even though grain size of SPC poly-Si is 0.2~2 μm, the electrically effective grain size is 100~500 Å. The small effective grain size relative to TFT channel dimension can result very uniform TFT characteristics due to reduction of grain size effect. In spite of grain defects, optimization of processes and device structures can achieve the TFT characteristics with V_t as low as ~2 volt and S slope as low as ~0.5 V/dec.

Recently, the advanced metal-induced crystallization, referred to *A-MIC,* such as super grain silicon (SGS) and Nanocap-Assisted Crystallization(NAC) have been reported [3]. Usually, MIC process is conducted for long time (~hrs) at low temperatures around 600°C. However, high temperature MIC process using FE-RTP enhances the MIC kinetics, thus, throughput. Currently, FE-RTP produces MIC poly-Si at 8~12 Gen. 4 glasses per hour.

Another important advantage of FE-RTP process is a quality of MIC poly-Si. Fig. 4 shows the comparison of the microstructures of MIC poly-Si at 600°C and 750°C. The apparent structure is the Ni silicide net-works which are formed after impingement of MIC lateral growth. High temperature gives a large silicide net-work with a low number density of silicides. Since the Ni silicide acts as a source of leakage current, high temperature MIC results superior TFT characteristics with low leakage current.

The uniform temperature control is essential to obtain a uniform MIC poly-Si. FE-RTP system, which has good temperature uniformity at process as well as heating/cooling stage, can produce uniform MIC poly-Si over large glass.

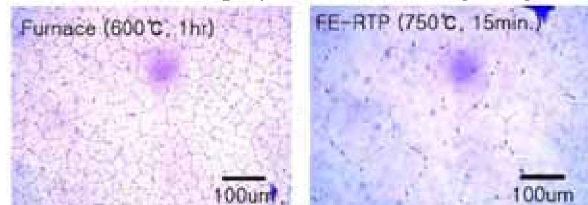

Fig. 4. Optical micrographs showing microstructure of MIC poly-Si

MIC poly-Si shows TFT mobilities up to 150~200 cm^2/V.sec, enabling System-On-Glass level integrations.

Thermal oxidation for gate oxides

Quality of gate oxide is known to be important in TFT characteristics. While PECVD-deposited oxides are commonly used as a gate oxide, thermal oxidation gives the best gate dielectric characteristics. In-line module process (IMP) of FE-RTP system can enable a sequential thermal oxidation following poly-Si crystallization. Fig. 6 shows the example of wet oxidation after crystallization. Pyrogenic H_2O oxidation at 700~800°C gives the oxidation rate high enough for real production. High quality gate oxide with low oxide and interface states can be obtained. Another advantage of thermal oxidation is the reduction of the intra-granular defects in SPC poly-Si, as shown in Fig. 7. It has been reported that oxidation enhances the defects annealing kinetics. Therefore, SPC poly-Si combined with thermal oxidation can give high performance TFTs, similarly to high temperature poly-Si TFTs (HTPS).

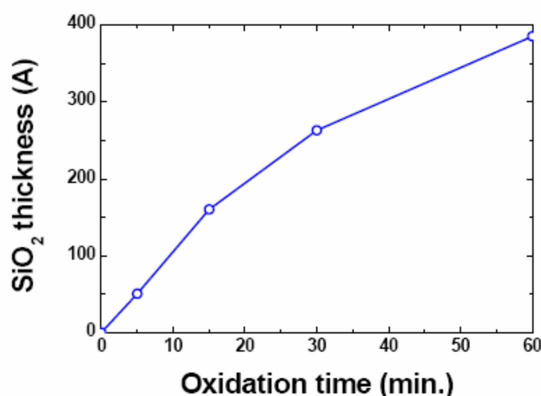

Fig. 5. Oxide thickness vs. oxidation time for wet oxidation at 750°C.

Rapid thermal pre-compaction

Frequently encountered problem in high temperature TFT process is the glass shrinkage. Substantial glass shrinkage up to 500~700 ppm occurs after high temperature glass heat treatment.

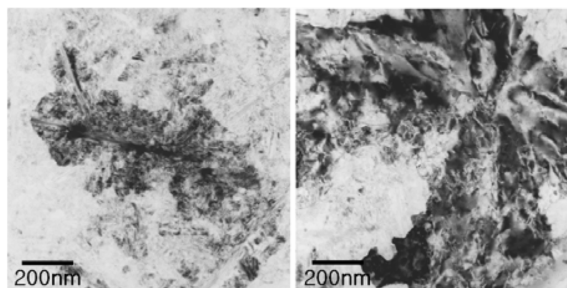

Fig. 6. TEM micrographs showing grain structures; a) SPC poly-Si and b) SPC and wet oxidation.

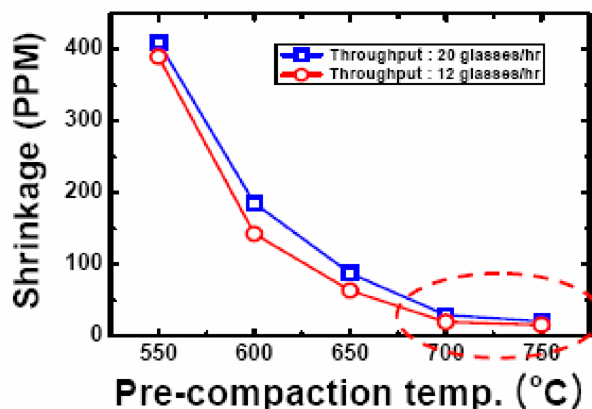

Fig. 7. Shrinkage value of pre-compacted glasses after FE-RTP SPC process at 750°C

Since excessive shrinkage causes pattern misalignment, the shrinkage should be controlled within 10~20 ppm. While the shrinkage is not a problem in most top-gate TFT structures, where TFT process starts with crystallization of blanket a-Si films, crystallizations or gate oxidations without shrinkage problem will allow more diverse choices of TFT structures and process recipes.

One way to solve the shrinkage problem is the pre-compaction of glass prior to TFT fabrications. Normally, the pre-compaction process is carried out at low temperatures around 550~650°C, and the pre-compacted glass still shows shrinkage problem at the process temperature (700~800°C) higher than that of the pre-compaction.

The degree of pre-compaction is determined by pre-compaction temperature and/or the cooling

rate of glass after pre-compaction. The high temperature pre-compaction and in-line control of cooling rate in FE-RTP system enables rapid thermal pre-compaction. Fig. 8 shows the shrinkage values after SPC process at 750°C for various pre-compaction temperatures. The glasses pre-compacted above 700°C shows the shrinkage less than 20 ppm after SPC process. Therefore, FE-RTP system can provide a solution to achieve SPC process without shrinkage problem.

Compatibility with a-Si TFT lines

As mentioned, poly-Si TFT production using a-Si TFT lines can reduce the production cost significantly for most TFT makers. Compatibility of SPC (or A- MIC) poly-Si process with a-Si facilities depends on the details of device structures and target products. However, most of process tools in a-Si lines can be used in SPC-poly-Si process. For example, the PECVD system and the process conditions used for a-Si deposition in a-Si TFT lines can be used for a-Si precursor deposition for poly-Si crystallization. This is not true in laser-crystallization due to hydrogen eruption problem.

Another issue in the compatibility is the access of equipments processing large glass substrate in the current a-Si lines. The FE-RTP system utilizes the two-dimensional heat flow (e.g., upper and lower planar heat flow) with multi-zone controls. This heating method ensures the thermal uniformity for larger glass size. The FE-RTP system for Gen 5 glass is under development and will be available by the end of 2006.

3. Conclusion

FE-RTP system provides the unique heat treatment methodology of sequential furnace and field-enhanced rapid thermal processes. FE-RTP system allows viable process options such as crystallization, thermal oxidation, and rapid pre-compaction. The FE-RTP system produces uniform poly-Si glass panels at low cost and high productivity by various solid state crystallization including SPC, MIC, and A-MIC. We believe that high uniformity of large poly-Si panels will provide the solution to the successful developments of AMOLED and LTPS LCD display manufacturing. Also, the process and equipment compatibility with a-Si TFT lines will open the possibility of production of poly-Si backplanes using a-Si lines, resulting reduction of production cost.

4. References

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