# Analysis of transport properties of SLS polysilicon TFTs

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**Abstract** An investigation of the transport properties of polysilicon TFTs, using sequential laterally solidified, SLS, material, is presented. This material has a location controlled distribution of grain boundaries, GBs, which makes it particularly useful for the analysis of their influence on the performance of polysilicon TFTs, and to address the issue of the role of spatially localised trapping states. The experimental results were analyzed by using numerical simulations, and the effective medium approximation was compared with a discrete grain model.

## 1. Introduction

Since the introduction of excimer laser annealing (ELA) polycrystalline silicon (polysilicon) thin film transistor (TFT) performance has been greatly improved, thus making possible system-on-panel applications [1]. However, the laser crystallisation process still presents issues of throughput, uniformity and process window size. An improved laser crystallisation technique has been proposed [2], called sequential lateral solidification (SLS), which promises to address these issues. In contrast to the conventional ELA process, which produces small diameter grains of ~300nm, the SLS technique can produce grains of almost arbitrary length (from microns to centimetres). They are also very narrow (~100-500nm), with sub-grain boundaries at this pitch. Hence the properties of this material can be highly anisotropic.

Several studies of devices fabricated in this material have already been reported [3-7], including the observation of carrier mobility anisotropy. However, these evaluations were limited, and in the work presented below we extend these studies to include measurements of the density of states (DOS), and the effect of an individual grain boundary orthogonal to carrier flow in the transistor channel.

The SLS samples have also been used for the investigation of issues related to the precise role of grain boundaries. For instance, many device simulation studies of poly-Si have ignored the presence of grain boundaries (GBs) as localised charge trapping sites, and have successfully modelled device behaviour using a spatially uniform density of trapping states [8]. On the other hand, there are studies which suggest that GBs have to be invoked to successfully simulate the low output impedance of poly-Si TFTs [9-13].

In the absence of a consensus on the appropriate way to electrically characterize the trapping states in poly-Si, the unique properties of SLS material have enabled us to address this problem.

## 2. Experimental

The transistors used in this work employed a non-self-aligned (NSA) architecture. The a-Si:H precursor film, 40 nm thick, was deposited at 250°C onto Corning glass 1737 substrates capped with $SiO_2$ and thermally dehydrogenated at 450°C prior to crystallisation. The source and drain regions were ion implanted with phosphorus before crystallisation. The SLS crystallisation was carried out by micro-translating the sample over an area of ~7 x 8mm$^2$, producing crystallites ~7mm long, with a sub-grain boundary pitch, in the orthogonal direction, of ~300nm [3]. Further details of the crystallisation procedures are beyond the scope of this paper and can be found in ref. [3]. The gate oxide was deposited by PECVD at 300°C, using $SiH_4$ and $N_2O$ to a thickness ($t_{ox}$) of 40 nm. The device channel was arranged in order to have the current flowing parallel or perpendicular to the sub-grain boundaries (see Fig. 1).

Fig. 2 shows the transfer characteristics for both n-and p-channel devices with channel length L=6 μm and width W=50 μm. It can be noted that the n-channel TFTs

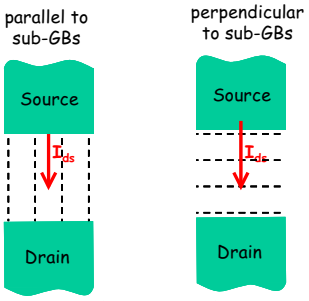


Fig. 1: Schematic of the device channel arrangement

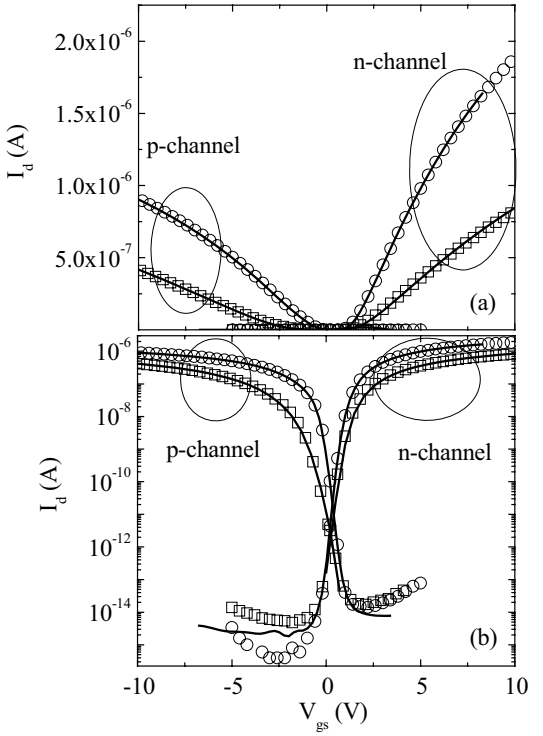


Fig. 2: Transfer characteristics, measured at $V_{ds}$=0.1 V, for both n- and p-channel TFTs fabricated with the drain current flow parallel (circles) and perpendicular (squares) to sub-GBs. Also shown are the simulated characteristics obtained by using the effective medium model (solid lines).

show almost identical characteristics for the two orthogonal current flow directions, apart from the already well established carrier mobility anisotropy, which is discussed further below. For current flow orthogonal to the sub-GBs, the subthreshold slope, S, values remained unchanged in the n-channel TFTs, indicating that the trapping properties of the material are determined just by the total trapping state density within the channel, irrespective of the direction of current flow (in sharp contrast to the carrier mobility anisotropy). The p-channel samples showed some anisotropy in S, which is more difficult to understand, and would suggest that the

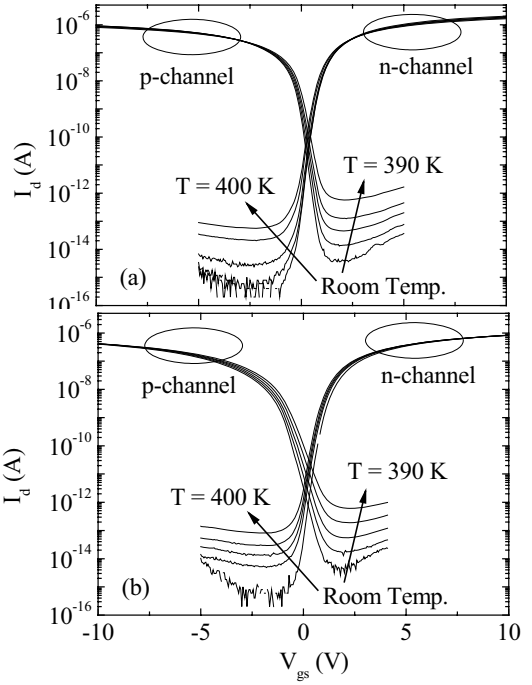


Fig. 3: Transfer characteristics, measured at $V_{ds}$=0.1 V and different temperatures, for both n- and p-channel TFTs fabricated with the drain current flow parallel (a) and perpendicular (b) to sub-GBs.

anisotropic hole transport properties are also affecting the sub-threshold characteristics.

Field effect mobility for n-channel devices was 205 and 80 $cm^2/Vs$, for parallel and perpendicular current flow respectively, while for p-channel devices it was 85 and 40 $cm^2/Vs$, for parallel and perpendicular current flow respectively. The estimated ratio between perpendicular and parallel average mobility values is 0.39 and 0.47 for n- and p-channel respectively, showing that carrier flow across the sub-GBs has a strong impact on the field effect mobility. It should be also pointed out that mobility ratios show some scatter in SLS devices, reflecting the present variability of the final grain structure [3-7].

In order to clarify the microscopic role of the sub-GBs on the transport properties, we have performed measurements of the transfer characteristics at different temperatures, for both n- and p- channel devices in the parallel and perpendicular configurations. In Fig. 3 the transfer characteristics at different T are reported and the drain current activation energies, deduced at constant Vg, are shown in Fig. 4.

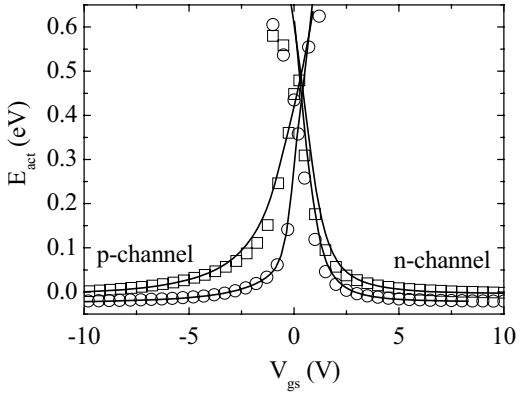


Fig. 4: Drain current activation energy, extracted from the data shown in Fig. 3, vs gate voltage, for devices with the drain current flowing parallel (circles) or perpendicular (squares) to sub-GBs. Also shown are the activation energies obtained from simulated characteristics by using the effective medium model (solid lines).

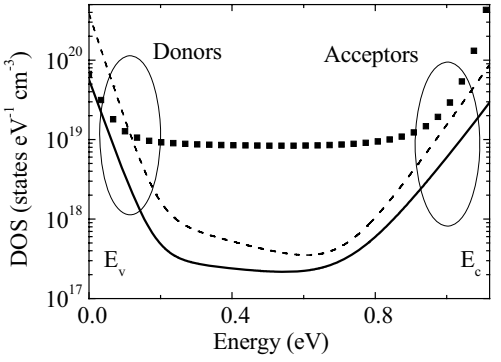


Fig. 5: Density of states (DOS) extracted by using the effective medium approximation and coupling both n- and p-channel characteristics for devices with the drain current flowing parallel (solid line) or perpendicular (dashed line) to sub-GBs. Also shown is the grain boundary DOS obtained using the discrete grain modelling for the device with the drain current flowing perpendicular to sub-GBs (filled squares).

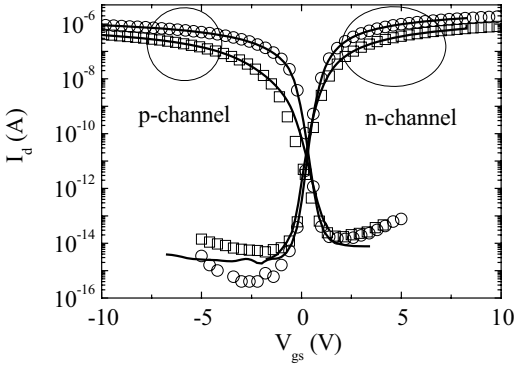


Fig. 6: Transfer characteristics, measured at Vds=0.1 V, for both n- and p-channel TFTs fabricated with the drain current flow parallel (circles) and perpendicular (squares) to sub-GBs, compared with the simulated characteristics obtained by using the discrete grain model (solid lines).

## 3. Numerical simulations: effective medium approximation

As already shown [7], by using the effective medium approximation, with a set of optimised parameters for the density of states (DOS) and impact ionisation parameters, it is possible to precisely reproduce the polysilicon SLS TFT characteristics in all their features. Iterative curve fitting was carried out on the transfer characteristics of both n and p-channel TFTs, with the DOS as an adjustable parameter, to achieve a consistent fit, which yielded a continuous DOS across both halves of the band gap. The fitted transfer characteristics are shown in Fig. 2 for the n- and p-channel TFTs and the resulting DOS values are shown in figure 3. For the SLS TFTs, very similar trapping state distributions were found in the upper half of the band gap for both carrier flow directions. In the lower half of the band gap, higher DOS values are recorded in the samples where carrier flow was perpendicular to the sub-GBs. This is consistent with the higher subthreshold slope in these TFTs.

We note that, in the case of devices with current flow parallel to sub-GBs, the current flows inside the grains and, therefore, the extracted DOS is representative of the in-grain defect density. In the case of devices with current flow perpendicular to sub-GBs, it was possible to reproduce the effect of the sub-GB on the transport properties by reducing the carrier mobility and by increasing the DOS (see Fig. 5). In this respect, the increased DOS can be regarded as an artefact of the current flow across the sub-GBs, where a higher defect density is expected.

By using the DOS illustrated in Fig. 5 and the temperature dependence of the field effect mobility, extracted from the experimental data, we simulated the drain current at different temperatures and evaluated the activation energies, similarly to that done for the experimental data. In Fig. 4 a comparison between activation energies deduced from both experimental and simulated data is shown. We can clearly see that the activation energy for the p-channel is perfectly reproduced while in the case of the n-channel we found that the activation energy from the simulated curves slightly overestimate the experimental one in the subthreshold region. Nonetheless, the overall agreement

remains very good.

In addition, the effective medium approximation has been shown to satisfactorily describe the SLS device output characteristics [7], thus confirming the ability of this approach to fully reproduce the SLS device characteristics.

## 4. Numerical simulations: discrete grain model

In order to get some more physical insight in the transport properties of the SLS devices we also investigated by numerical simulations schematizing the polycrystalline material as a sequence of small crystallites connected by grain boundaries. This model was originally proposed to explain the conductivity in polysilicon, assuming that transport properties are controlled by carrier trapping at grain boundaries [14]. Transport properties are derived assuming that crystallite conductivity is much higher than that through the grain boundary and that the main mechanism controlling the current flow across grain boundaries is thermionic emission.

Successively, more complete transport models in polycrystalline materials have been proposed, combining thermionic emission across the grain boundary barrier with drift-diffusion in the grain regions [15, 16]. In particular, the transport mechanism is actually thermionic or diffusive depending upon the relative values of the collection velocity, $v_c$, and the velocity $v_d=v_D/(D1+D2)$, where $v_D$ is the Debye velocity and D1 and D2 are Dawson functions of $(E_{b1}/KT)^{½}$ and $(E_{b2}/KT)^{½}$ respectively, with $E_{b1}$ and $E_{b2}$ being the barrier heights for the grains located at the left and right of the grain boundary [15, 16]. If $v_c>>v_d$ drift-diffusion dominates the transport process while if $v_c<<v_d$ thermionic emission predominates. However, considering the thermionic-diffusion current expression [15, 16], we can see that in both thermionic or drift-diffusion limit the current density will be an exponential function of barrier height and only the pre-exponential term depends upon the dominant transport mechanism. Therefore, whatever theory is used the current density overcoming the barrier will be an exponential function of the barrier height and only the pre-exponential term will be affected. Hence, a numerical model based on drift-diffusion will properly interpret the essential dependence of current density vs potential distribution in simulated device. Several authors [9-13] have adopted this approach to investigate the electrical characteristics of polysilicon TFTs, assuming that grain boundaries behave as interfaces where a large density of acceptor-like (located in the upper-half of the bandgap) and donor-like (located in the lower-half of the bandgap) states are included. The grains were considered as crystallites of regular size that may [10-13] or may not [9] contain intragrain defects, while grain boundaries can have finite thickness [11, 12] or can be approximated as two-dimensional interfaces (zero thickness) [9, 10, 13].

In order to simulate the transport in perpendicular TFTs, the active layer was approximated as a sequence of 0.3 μm grains separated by GB regions, having a finite thickness (2 nm). From the effective medium analysis of parallel TFTs, we could estimate the DOS and carrier mobility of the grains, as the conduction is occurring inside the grains. In addition, due to limitations in the number of the nodes in the simulation grid, the device channel length was scaled down to 1.5 μm, thus including a total of 5 grains. Extensive numerical simulations conducted at different channel lengths showed that for this channel length short channel effects are still negligible, thus allowing a scaling of the characteristics for longer channel lengths.

Numerical simulations were performed with the program DESSIS, using the drift-diffusion model. Having fixed the DOS and carrier mobility for the grains, the DOS and the carrier mobility for the GB were adjusted by fitting the experimental data for the perpendicular TFT. In Fig. 5 the DOS for the GB is also reported and can be compared with the one deduced for the parallel TFT and representative of the in grain DOS. The GB carrier mobility giving best results were 2.2 $cm^2/Vs$ and 1 $cm^2/Vs$ for electrons and holes, respectively. The device characteristics are reported in Fig. 6 and compared with the experimental data: as can be seen also with the discrete grain approximation it is possible to nicely reproduce the data. In Fig. 7 the extracted activation energies are compared with the experimental data and a good agreement is also found.

By using this analysis it is possible to address the issue of the different activation energy observed between parallel and perpendicular TFTs and see whether this difference could be related to the presence of barrier heights induced by GBs. In particular, in Fig. 8 is reported the activation energy difference between parallel and perpendicular TFTs, $\delta E=E_{//} - E_{\perp}$, extracted from the data reported in Fig. 7. To clarify if δE arises from the

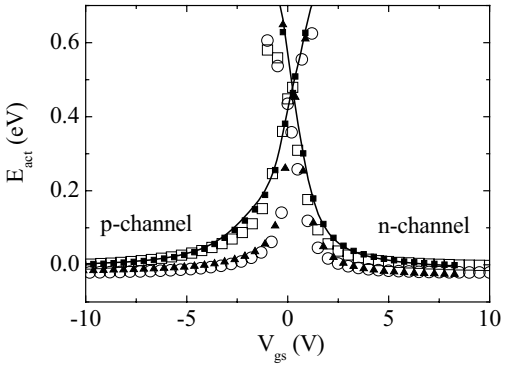


Fig. 7: Drain current activation energy, extracted from the data shown in Fig. 3, vs gate voltage, for devices with the drain current flowing parallel (circles) or perpendicular (open squares) to sub-GBs, compared with the activation energies obtained from simulated characteristics by using the discrete grain mode model (solid lines). Also shown the activation energy of the product of carrier mobility times the carrier density, integrated in the grain (triangles) and in the grain-boundary (filled squares).

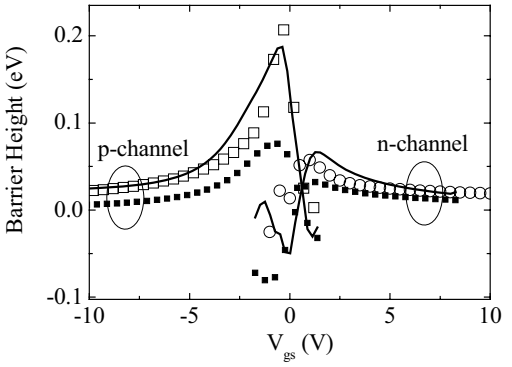


Fig. 8: Activation energy difference, between parallel and perpendicular TFTs, vs gate voltage: experimental data (open squares and circles); simulated data by using the discrete grain model (solid lines). Also shown is the barrier height extracted from the potential profiles shown in Fig. 9 (filled squares).

presence of the barrier height introduced by the presence of the GB, we analysed the potential distribution along the channel (see Fig. 9) and from this we evaluated the barrier height as the potential difference between the centre of the GB and the centre of the grain. The extracted values for the barrier heights are reported in Fig. 8 and we can clearly see that the barrier heights introduced by the GBs are much lower than the δE values.

We have analysed the product of carrier mobility times the carrier density, integrated within the GB and the grain, to determine their respective temperature dependence. In Fig. 7 are reported the activation energies for these two quantities and we can see that the average μxn product in

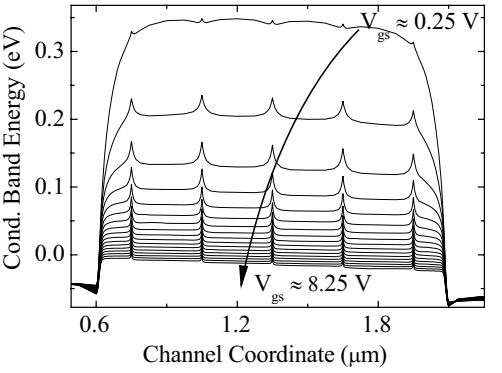


Fig. 9: Potential profiles, extracted from numerical simulations by using the discrete grain model, for different applied gate voltages. The cut-lines are taken along the insulator-semiconductor interface.

the grain perfectly agrees with the full simulation of the parallel TFT, and the activation energy of the average μxn product in the GB also agrees with the activation energy of the full simulation with discrete grains, reproducing the perpendicular TFT. Therefore, we conclude that the current, as well as its temperature dependence, in the perpendicular TFT are controlled by the resistance of the GB regions.

## 5. Conclusions

An investigation of the transport properties of polysilicon TFTs, using sequential laterally solidified, SLS, material, is presented. This material has a location controlled distribution of grain boundaries, GBs, which makes it particularly useful for the analysis of their influence on the performance of polysilicon TFTs, and to address the issue of the role of spatially localised trapping states. The experimental results were simulated by using the effective medium approximation and a discrete grain model. The effective medium approach showed that depending upon the current flow, parallel or perpendicular to the GBs, different density of states (DOS) are needed to reproduce the experimental data. Nevertheless, most aspects of TFT performance could be accurately simulated using a spatially uniform distribution of states. From the discrete grain model a deeper physical insight was achieved and the role of GBs was better clarified. In particular, it is found that the transport properties of devices with the current flow crossing GBs are controlled by the resistance of the GBs, determined by the carrier concentration and mobility in the GB, rather than by the barrier height formed between grains.

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