Dependence of Self-heating Effect on Width/Length Dimension in p-type Polycrystalline Silicon Thin Film Transistors

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Abstract

Self-heating induced device degradation and its width/length (W/L) dimension dependence were studied in p-type polycrystalline silicon (poly-Si) thin film transistors (TFTs). Negative channel conductance was observed under high power region of output curve, which was mainly caused by hole trapping into gate oxide and also by trap state generation by self-heating effect. Self-heating effect became aggravated as W/L ratio was increased, which was understood by the differences in heat dissipation capability. By reducing applied power density normalized to TFT area, self-heating induced degradation could be reduced.

1. Introduction

Low-temperature polycrystalline silicon (LTPS) thin-film transistor (TFT) is widely attracted for the integration of so-called system on panel (SOP) due to its high mobility and low threshold voltage (V_{th}). Improvement of TFT performance is one of the requirements to achieve value-added SOP. Sequential lateral solidification (SLS) process is attracting considerable attention for its ability to enlarge grain size to obtain better device performance, and for its capability to control grain boundary (GB) position to obtain better device uniformity than other crystallization method [1].

Improvement of device performance, however, generally shows a trade-off with device reliability. Degradation caused by self-heating is one of the critical reliability issues of poly-Si TFTs [2]. TFTs are fabricated on glass substrate having lower thermal conductivity, which reduces self-heating induced heat dissipation to the substrate. The self-heating effect is known strongly depend on TFT area, thus heat dissipation capability [3]-[4].

In this paper, self-heating induced device degradation and its W/L dimension dependence were studied in p-type SLS poly-Si TFTs. The dimension dependence of self-heating effect shown in this paper will give an insight for designing compact-designed SOP with increased reliability.

2. Results

Output characteristic and its output conductance of TFT with a dimension of W/L = 120/6 ㎛/㎛ are shown in Fig. 1. Negative output conductance was observed only in the curve of V_{gs} = -15V, which is understood by the self-heating effect [5]. Carrier scattering increases as temperature rise by self-heating effect, as a consequence mobility is decreased eventually led to drain current reduction in output curve [6].

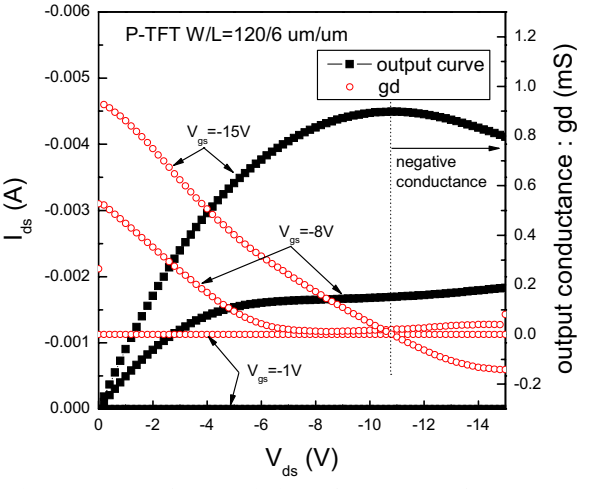

Fig. 1. Output characteristic and output conductance (gd) of P-TFT with W/L = 120/6 ㎛/㎛. Negative conductance was observed under high power operation of V_{gs} = -15V curve.

To find out self-heating effect induced degradation, transfer curves were compared. Fig. 2 shows variations of transfer curves as a function of bias condition under high drain current stress (HDCS), where V_{gs} was equally biased with V_{ds} and stress duration was 60 sec regardless of bias condition. Virgin TFTs with negligible differences (standard deviation of V_{th} = 44 mV) in initial characteristics were measured for each bias condition. Negative shift and increase of OFF current in transfer curve explained that hole trapping was major cause of device degradation induced by self-heating effect [7]. Degradations of sub-threshold slope due to deep level state generation were continuously enhanced by increased bias condition with a degradation slope normalized to applied power of 1.1 V/(decade · Watt), where the applied power was defined by $I_{ds} \times V_{ds}$ under HDCS. Drastic degradations of ON current were observed over around 10 nA of I_{ds} caused by shallow level defect state generation as bias condition was increased. Not only deep level but also shallow level defect generation was occurred in the self-heating induced degradation, which could be explained by Si-H bond breaking induced degradation [3].

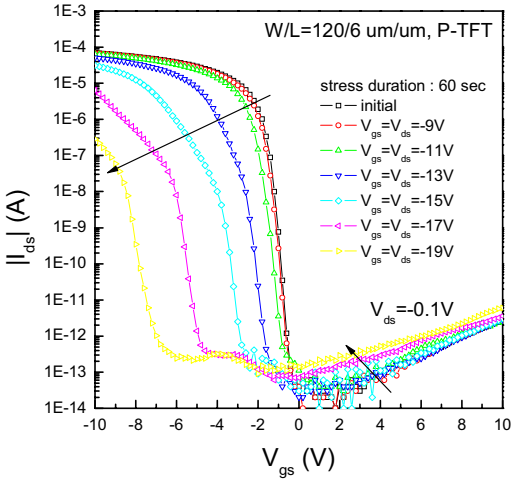

Fig. 2. Variation of transfer characteristics with V_{ds} = -0.1V as a function of applied HDCS condition, where V_{gs} was equally biased with V_{ds} and stress duration was 60 sec, regardless of the bias condition.

W/L dimension dependence of self-heating induced degradation was studied with respect to applied bias and applied power under HDCS. Fig. 3 shows comparison of ΔV_{th} as a function of applied bias and applied power density normalized to TFT area, where W/L of TFT was split with constant gate length of 6 ㎛. ΔV_{th} was severed as stress condition was increased and also as W/L ratio was increased.

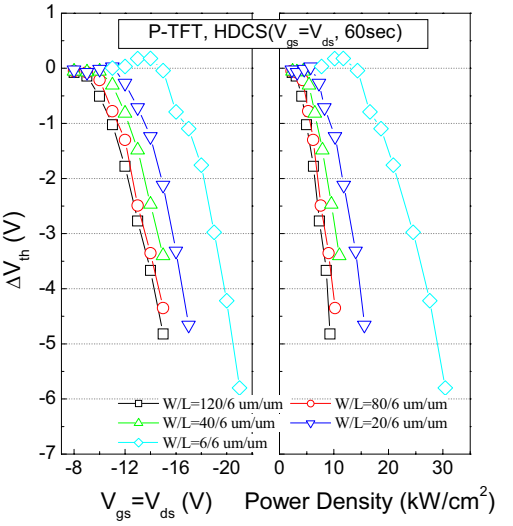

Fig. 3. Threshold voltage variation (ΔV_{th}) as a function of applied bias and applied power density normalized to TFT area under HDCS. The stress duration was 60 sec regardless of the bias condition. Applied power was defined by $I_{ds} \times V_{ds}$.

To find out detailed relation between self-heating induced degradation and W/L ratio, the power density causing 1V of ΔV_{th} was measured and shown in Fig. 4. The power density inducing 1V of ΔV_{th} was in inverse proportion to W/L ratio. Self-heating effect was enhanced as W/L ratio was increased, considering the power density is normalized to TFT area. Which could be understood by the difference in heat dissipation capability between large- and small-width TFTs. The heat dissipation length along gate direction is longer for large-width TFT than that of small-width TFT, which brings difficulty in heat dissipation as width of TFT is increased. As a consequence, self-heating induced degradation is severed as W/L ratio is increased. Satoshi Inoue, *et al.* compared maximum temperature between large- and small-width TFTs under high power condition, where large-width TFT showed higher temperature than that of small width TFT [8], which support the explanation of heat dissipation difference. For more detailed study, multi-channel TFT was compared to single-channel TFT

with respect to self-heating induced degradation. The multi-channel TFT was designed to have same W/L dimension of 120/6 ㎛/㎛, but had 25 % of increased TFT area by adopting divided channel scheme compared with single-channel TFT [3].

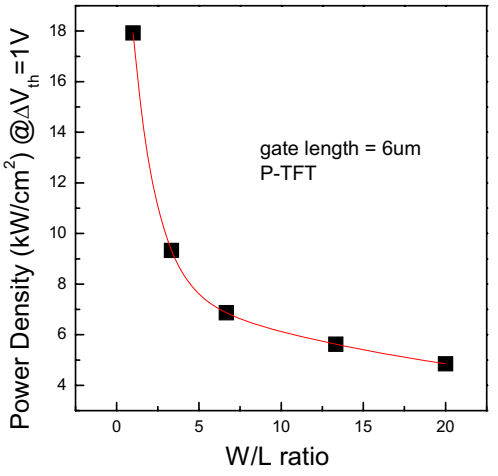

Fig. 4. Comparison of power densities causing 1V of ΔV_{th} as a function of W/L ratio. Gate length was 6 ㎛ regardless of W/L ratio.

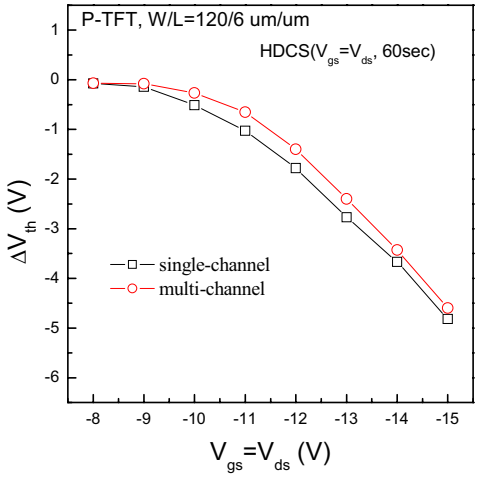

Fig. 5. Comparison of ΔV_{th} between single-channel and multi-channel TFTs with a same W/L dimension of 120/6 ㎛/㎛ as a function of applied bias under HDCS. The multi-channel TFT has 25 % of increased TFT area by adopting divided channel scheme compared with single-channel TFT.

Fig. 5 shows the comparison of ΔV_{th} between single-channel and multi-channel TFTs as a function of applied bias condition under HDCS. Multi-channel TFT had better immunity to self-heating effect, which was from the reduced applied power density by increasing TFT area.

3. Conclusion

Self-heating induced degradation and its dimension dependence were studied in p-type poly-Si TFTs. Self-heating effect led to negative shift of transfer curve by hole trapping, and degradation of sub-threshold slope and ON current by Si-H bond breaking. The self-heating induced degradation was aggravated as W/L ratio increased, which was explained by the differences in heat dissipation capability. The heat dissipation capability was reduced as width of TFT increased, considering heat dissipation path along gate direction is longer for large-large width TFT. Reduced self-heating effect in multi-channel TFT adopting divided channel scheme was due to lowered applied power density by increasing TFT area, which will give an insight in designing SOP considering both of reliability and narrow bezel of the panel.

4. References

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