SLS Crystallized Poly-Si TFT Technology

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Abstract

The Process technology for uniform SLS poly-Si and performance enhancement of furnace activated poly-Si TFTs are reported. By strictly optimizing SLS optics, threshold voltage variation in pixel TFTs was remarkably decreased and the non-uniformity such as SLS shot mark was removed. Optimized doping process for low sheet resistance and passivation annealing are critical for the enhancement of device performances.

1. Introduction

Polycrystalline Si (poly-Si) TFT has been widely used as pixel switching- and circuit-device for advanced mobile liquid crystal display (LCD) and system-on-glass (SOG) or system-on-panel (SOP). Higher carrier mobility of poly-Si TFT compared with that of a-Si TFT, makes it possible to integrate external driver ICs, other peripheral circuits, memory and ultimately CPU on the glass [1]. High performance poly-Si TFT is required to enhance circuit integration level and improve the quality of displays. In order to enhance the performances of poly-Si TFT, so many crystallization technologies for high quality poly-Si film have been developed. Among various crystallization technologies, sequential lateral solidification (SLS) [2-4] has attracted many attentions because of its productivity, superior crystalline quality, flexibility for obtaining various microstructures and wide process range. Previous reports demonstrate that SLS crystallization is attractive for high performance TFT[5] and SOG[6], compared with conventional excimer laser annealing (ELA) method. In order to enhance the device performances, the laser annealing for dopant activation is widely used.

Our approach is the furnace activation method because we considered that the furnace annealing is more cost-effective and advantageous for the uniformity than the laser annealing.

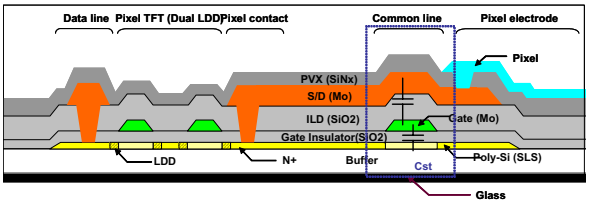


Fig. 1. Schematic cross-section of TFT.

In the development of SLS crystallization and furnace activated poly-Si TFTs, it is required to control the non-uniformity such as "SLS shot mark" and enhance the TFT performances.

In this paper, we described our approaches to the above issues and development results of performance enhancement for CMOS TFTs, and SLS shot mark removal.

2. Process sequence and TFT structure

8 mask CMOS LTPS process was applied to fabricate the poly-Si TFT. SiO2 buffer layer and a-Si film (500 Å) were deposited and the a-Si was crystallized by 2 shot SLS after dehydrogenation at 500 ℃. In order to adjust the Vth, active poly-Si was doped by Boron atoms. After poly-Si patterning to active islands, SiO2 gate insulator film and gate (Mo) material layer were deposited and followed by gate Mo patterning. S/D contact region of N-channel TFT (NTFT) and P-channel TFT (PTFT), and LDD (Lightly Doped Drain) region were doped by using an ion shower doping machine. Dopant activation annealing was carried out in a furnace at 500 ℃ after inter-layer dielectric (ILD) film deposition. Then, S/D contact holes were formed and S/D metal layer deposition and S/D patterning was performed. Then, SiNx passivation layer deposition and passivation annealing were performed. After via hole formation, pixel electrodes were patterned. A schematic cross-section of TFTs is shown in Fig. 1.

3. Process technology and TFT characteristics

3.1. SLS : Process design and uniformity

Figure 2 is a mask pattern of slit-type n-shot SLS and microstructure evolution. The mask pattern consists of slit-arrays. The width of slit is Y1 and that of masking region is Y2. Y1 and Y2 are limited above the optical resolution of 1.5 um. In order to avoid nucleation phenomenon, Y1 is also limited above the lateral growth (LG) length. In n-shot process, previously formed poly-Si regions act as the seeds for the next shot and elongated to the final size L_T (targeted microstructure) by sequential lateral growth (SLG) of each shot. We derived the correlation between mask design parameter, process condition, and targeted microstructure [7]. Based on the correlation, we can design the SLS process and an example of the design is given in Fig. 3(a). At a given laser energy density, the LG length and upper boundary of Y1 are fixed. Thus, it is desirable to select the n-shot process scheme, having the Y1 and Y2 between the upper and lower bound. For example, if we would like to a grain size (L_T) of 9 um, at least 4 shot process is required because fine-grained poly-Si region is formed by nucleation process when n<4.

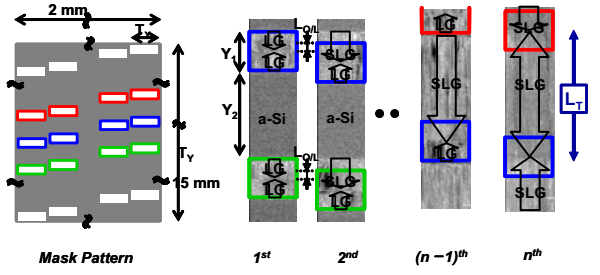


Fig. 2. A mask pattern and microstructure evolution of n-shot SLS.

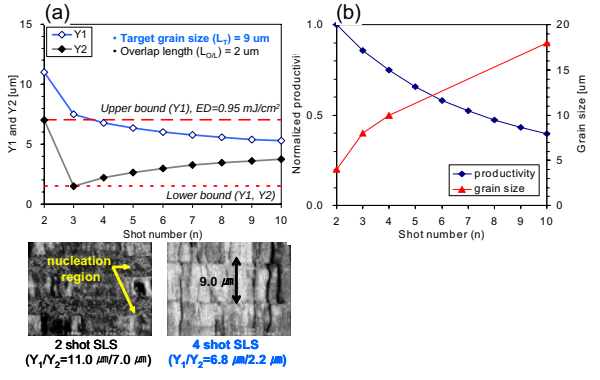


Fig. 3. n-shot SLS. (a) Diagram for the correlation between mask design parameters and n, and microstructure of 2 and 4 shot SLS (b) Productivity and grain size with n

Grain size and crystal quality can be improved by increasing the shot number and high performances of TFT are expected. However, the productivity decreases with n [Fig. 3(b)]. Thus, it is important to optimize the SLS processing method and design between the productivity and material requirements. Currently, our choice is 2 shot SLS.

The SLS beam of this work has the dimension of 2mm x 15mm which is relatively small compared with the larger area of glass substrate. In addition, there exists a laser energy variation in shot-to-shot. In addition, the energy profile within each shot is not perfectly flat and those of slits in the mask may be different from one another. Occasionally, non-uniform features emerge as “SLS shot mark” in the display area.

Figure 4(a) and (b) are gray scale images of a panel fabricated by a conventional 2 shot SLS. When the backlight is on while the TFTs are off [Fig. 4(a)], there is no non-uniformity in the display area. However, when the TFTs are on [Fig. 4(b)], sharp boundaries and white columns are observed. Particularly, the distance between these boundaries and columns is 15 mm, exactly fitted to the SLS beam dimension. According to our simulation, a wide variation of Vth in pixel TFTs causes the variation of feed through voltage (ΔVp) of pixel TFTs and finally emerges as the non-uniformity of transmittance in the display. Therefore, these results indicate that the features in Fig. 4(b) should be originated from the non-uniformity of pixel TFT characteristics, which is closely related with the SLS process.

As an approaching method for the SLS shot mark, “shot mixing method” [8,9] was proposed and successfully demonstrated with an active matrix organic light emitting display (AMOLED). However, that method needs a complicated SLS mask design and may decrease the throughput.

Our approach is to improve SLS laser beam uniformity by strictly optimizing the optics (lens, mirror, etc) of the SLS system. We used a conventional 2 shot SLS mask and thereby there is no decrease in the throughput. Anti-reflective (AR) coating on the SLS mask is also helpful for the uniform profile in the SLS beam dimension. After SLS optics tuning, we have improved the uniformity of SLS process and successfully fabricated the SLS shot mark-free panel as shown in Fig. 4(c).

The improvement of beam uniformity was also confirmed by comparing the Vth variation in whole pixel TFTs along the panel horizontal

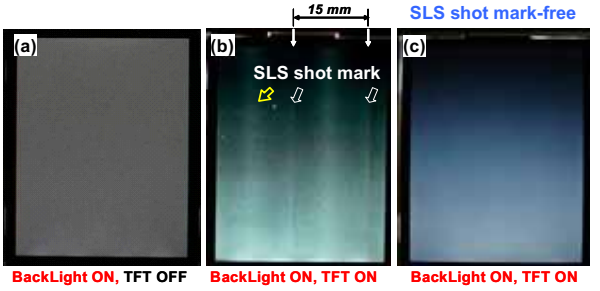


Fig. 4. Gray scale images obtained in the panel (a) and (b) before SLS beam tuning and (c) after SLS beam tuning.

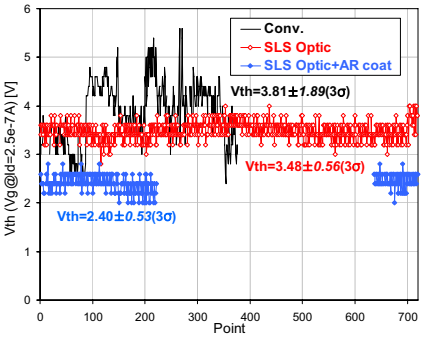


Fig. 5. Vth of pixel TFTs along a gate line in the panel. (a) Before SLS beam tuning (b) SLS beam tuning and (c) SLS beam tuning + AR film-coated SLS mask.

direction (gate line direction) before and after SLS process tuning. The Pixel TFT has a dual gate NTFT structure with W/L/LDD=4/(4+4)/1.5 um. In Fig. 5, we compared Vths measured from 720 pixel TFTs for three kinds of 2.2-inch QVGA panels. 3sigma of Vth was 1.89 V for the conventional panel. By SLS optics tuning, the 3sigma value was remarkably decreased to 0.56 V. It should be noted that for the case of SLS optic tuning and AR-coating SLS mask, the Vth variation was slightly improved from that of SLS optic tuning only. Thus, AR-coating on SLS mask may be helpful, but the optics is more critical for the SLS process uniformity.

3.2. Doping and activation

In order to enhance the device performances, low sheet resistance (Rs) of doped poly-Si film of S/D region is important as well as high quality of poly-Si and gate oxide. Figure 6(a) and (b) are Rs of doped poly-Si after 500 ℃-furnace activation as a function of acceleration voltage (Vacc) and dose, respectively. During the ion shower doping process, large amount of outgassing from photo-resist (PR) and the dose shift occurs [10,11]. These phenomena may deteriorate the Rs and

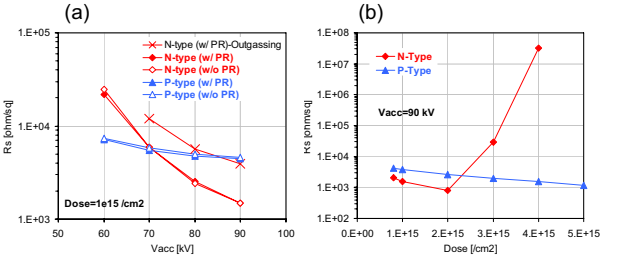
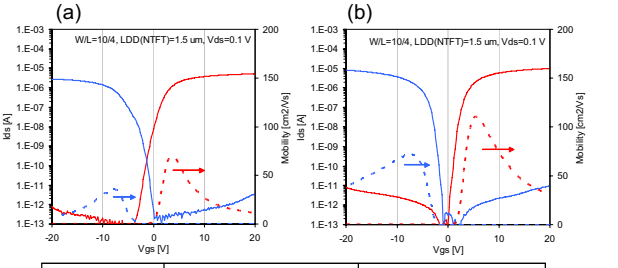


Fig. 6. Sheet resistance as a function of (a) acceleration voltage and (b) dose of doped poly-Si after the furnace activation at 500 ℃-2 hr.



	Large PR outgassing		Reduced PR outgassing	
	NTFT	PTFT	NTFT	PTFT
Vth [V]	1.65	-5.46	3.27	-4.14
Mobility [cm2/Vs]	69	36	110	72
Slope [V/dec]	0.42	0.47	0.35	0.40

Fig. 7. I-V characteristics and device parameters of the poly-Si TFT with different outgassing amount during the doping process. (a) large outgassing (b) minimized outgassing

uniformity. We revised the mask design and doping process to minimize the outgassing issues, and obtained Rs values comparable with those of doped poly-Si without PR. As compared in Fig. 7(a) and (b), the device performances can be improved with the reduced PR outgassing which is related with low Rs of doped poly-Si at the S/D region.

As the dose increases at a fixed Vacc, Rs decreases. However, Rs value abruptly increases when the dose is larger than 2e15 /cm2 for N-type doped Si. This is because the large doping damage at the elevated dose was not removed by the furnace annealing.

In order to adjust Vth for the symmetric CMOS characteristics, channel doping was applied with the dose under 5e11 /cm2.

3.3. Passivation and annealing

Passivation (PVX) layer (SiNx) deposition and subsequent annealing are also critical to enhance the TFT characteristics. Figure 8 shows the effect of PVX layer and annealing (passivation annealing) on the I-V characteristics. When there

is no PVX layer, the annealing effect on the TFT characteristics is small except the leakage current. As for the annealed TFT having the PVX layer, the device characteristics are remarkably improved. It is thought that the improved performances are related with the hydrogen-passivation of defect states after annealing since the PVX layer has a large amount of hydrogen.

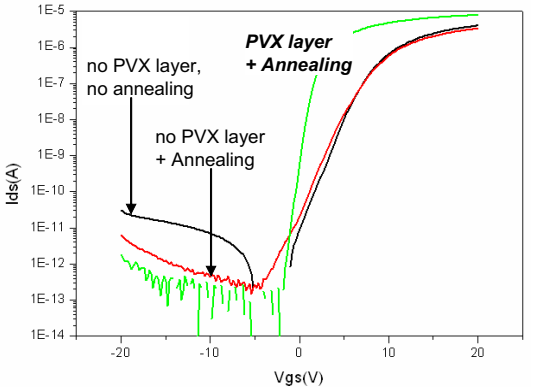


Fig. 8. The effect of PVX layer and subsequent annealing on the I-V characteristics of poly-Si TFTs.

4. Panel fabrication

A display image of 2.2-inch QVGA poly-Si panel with integrated gate driver and 3:1 DeMUX switching circuits is shown in Fig. 9

Parameter	Specifications
Glass	0.5t glass
Display size	2.2 inch (TN)
Resolution	qVGA (180 ppi)
Pixel number	240 x RGB x 320
Pixel pitch	46.5 ㎛ x 139.5 ㎛
Brightness [cd/m2]	250 (typ.)
Contrast ratio	300:1
Viewing angle (R/L/U/D)	45/45/15/30
Gray scale	64 gray (262k colors)
Color gamut	45 %
Driving voltage	(10 V / -5 V) / 4 V / 4 V (Vgate)/Vdata/Vcom
Driving method	Line inversion
Integrated circuit	Gate driver Source 3:1 DeMUX

Fig. 9. 2.2-inch QVGA display and panel specification.

5. Summary

We have developed SLS poly-Si TFT technology based on the device performance and productivity. Design and process scheme of n-shot SLS are derived. By strictly optimizing SLS optics in conventional 2 shot SLS scheme, the Vth variation of pixel TFTs and the display uniformity were remarkably improved. In order to enhance device performances of poly-Si TFT fabricated by ion shower doping and furnace activation, it is important to control the outgassing from photo-resist during the doping process. Additionally, passivation annealing is also critical to obtain high performances of poly-Si TFT.

6. References

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