ΔV_p Compensated TFT-LCD Pixel Structure for Ultra High Picture Quality Displays

Jun-Yong Song, Ung-Gyu Min, Jung-Hwan Choi, Min-Seok Shin, Seung-Yong Lee, and Oh-Kyong Kwon
Division of Electrical and Computer Engineering, Hanyang University,
17 Haengdang-dong, Seondong-gu, Seoul, 133-791, Korea
Phone: +82-2-2220-0359, E-mail: okwon7@chol.com

Abstract

In this paper, we proposed a novel TFT-LCD pixel structure to compensate ΔV_p, which is a maximum value of 1.82V in conventional pixel structure without compensation. We achieved a maximum value of 60mV in proposed pixel structure by integrating a dummy switch TFT in each pixel. The proposed TFT-LCD pixel structure with a remarkably reduced ΔV_p allows ultra high picture quality AMLCDs.

1. Introduction

TFT-LCDs stand in the spotlight of large size and high picture quality flat panel displays (FPDs) such as TV applications [1]. LCD TVs require that higher gray scale than 10-bit and higher resolution format than full-HDTV to share large portion of the TV markets in the future [2].

Although the TFT-LCD technology has been improved, there are still some problems to overcome. A voltage error, ΔV_p, which is also known as kick-back voltage is one of them. When a pixel TFT is turned off, the ΔV_p is induced to the pixel electrode. It leads to display picture quality deterioration such as flickers, shadings, and gray scale errors [2 - 4].

There were many efforts to reduce it by modifying the pixel structure and driving methods [4]. However, there are some problems such as complex gate driving waveforms, additional voltage levels, and constraints on scanning direction [2] [4].

This paper presents a novel technique to compensate the ΔV_p by adding a dummy switch TFT and a signal line. The dummy switch TFT which is driven by a simply inverted gate signal simultaneously gives an additional voltage rising on the pixel electrode when the ΔV_p is occurred. This additional voltage rising compensate the ΔV_p.

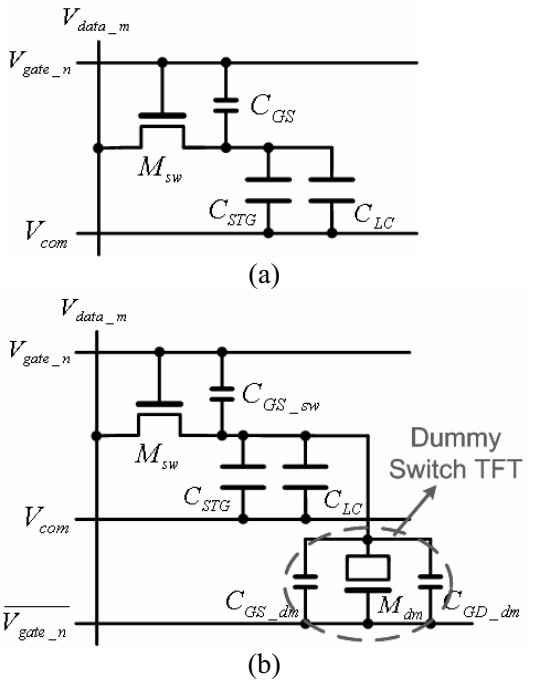


Figure 1. Schematic diagram of TFT-LCD pixel to calculate ΔV_p (a) conventional structure, (b) proposed structure.

2. Proposed Pixel Structure

The conventional and proposed schematic diagrams of TFT-LCD pixel to model the ΔV_p are shown in Figure 1(a) and (b), respectively, and the driving waveforms are shown in Figure 2(a) and (b) respectively. When the switch TFT (M_{sw}) is turned off by gate signal, the ΔV_p occurs to the pixel electrode. The ΔV_p is proportional to the parasitic capacitance between gate and source of the switch TFT (C_{GS}), and reciprocal to the summation of a storage capacitance (C_{STG}), C_{GS}, and the liquid crystal capacitance (C_{LC}) [4] as shown in Equation (1)

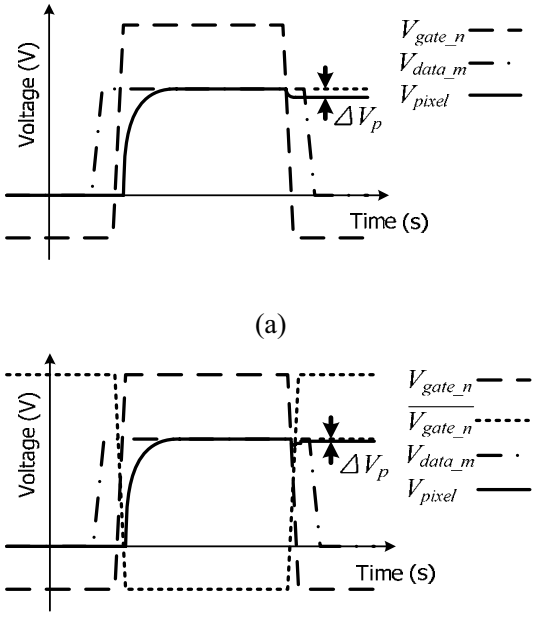


Figure 2. Driving waveforms (a) conventional structure, (b) proposed structure.

$$\Delta V_P = \frac{\Delta V_{gate\_n} \cdot C_{GS}}{\left[C_{GS} + C_{STG} + C_{LC}\right]}. \qquad (1)$$

Therefore, C_{GS} should be minimized and C_{STG} should be increased to reduce it. But, there is a limitation in reducing it because of the design rule and the aperture ratio. The ΔV_p is a function of C_{LC} which is dependent on data voltage [3]. Therefore, it is difficult to predict and remove the ΔV_p.

In the proposed pixel structure, there is an additional dummy switch TFT, M_{dm}, which is turned on by an additional signal line, $\overline{V_{gate\_n}}$, when M_{sw} is turned off. $\overline{V_{gate\_n}}$ signal can be simply generated by inverting the V_{gate_n} signal. Therefore, there is an additional voltage rising on the pixel electrode by dummy TFT switch which is expressed as Equation (2)

$$\Delta V_{P\_dm} = \frac{\Delta \overline{V_{gate\_n}} \cdot (C_{GS\_dm} + C_{GD\_dm})}{\left[C_{GS\_dm} + C_{GD\_dm} + C_{STG} + C_{LC}\right]}. \qquad (2)$$

By making C_{GS_dm} and C_{GD_dm} same as C_{GS}, i.e. ΔV_p is same as ΔV_{p_dm}, we can simply cancel out the ΔV_p.

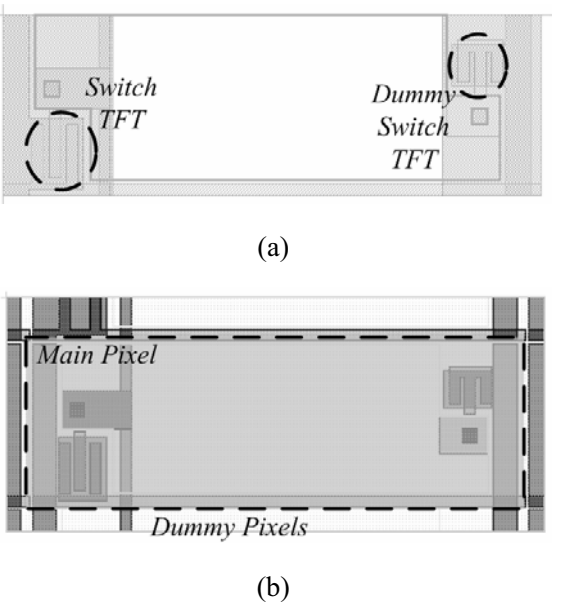


Figure 3. Layout of proposed pixel structure (a) simplified layout, (b) layout with dummy pixels.

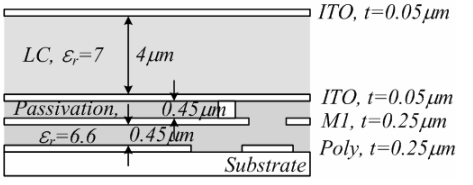


Figure 4. Cross section of the pixel with physical dimensions and dielectric constants.

C_{GS_dm} and C_{GD_dm} are determined by the paprasitic capacitance between dummy gate line and pixel electrode and the width of the M_{dm}. In order to minimize the ΔV_p in the proposed pixel structure, careful layout is very important.

3. Modeling of the Pixel Structure

We extract the parasitic capacitances from the layout using *Raphael* [5] and make the electrical models for the conventional and proposed pixel structures to accurately obtain the ΔV_p.

Simplified layout of the proposed pixel structure is shown in Figure 3(a). Because there is a parasitic capacitance between the pixel electrode and the gate line which contributes to C_{GS}, we must carefully draw the layout of the gate line, dummy gate line, metal 1, and ITO to match the capacitances

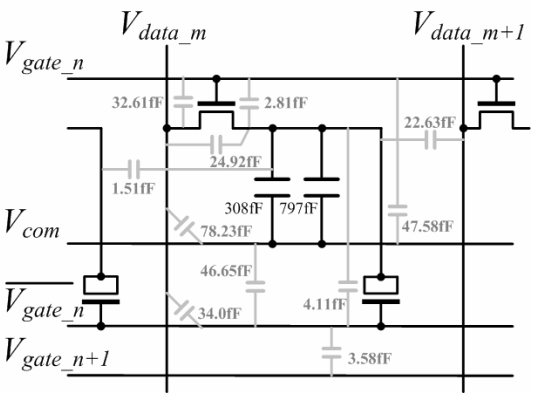


Figure 5. Schematic diagram with extracted parasitic capacitances.

between switch TFT and dummy switch TFT. We draw a 3-by-3 pixel array and capture the near region of the main pixel to model the effects of the neighboring pixels as shown in Figure 3(b). Cross section of the pixel with physical dimensions and dielectric constants are shown in Figure 4.

Schematic diagram with extracted parasitic capacitances is shown in Figure 5. The extracted parasitic capacitance between the gate line and the pixel electrode, and the dummy gate line and the pixel electrode are 2.81fF and 4.11fF, respectively. The extracted two parasitic capacitances are different in spite of the careful drawing.

4. Simulation of the Pixel Structure

We used 3-by-3 pixel array to simulate the ΔV_p. The simulation conditions are shown in Table 1. We applied a skew of 100ns between V_{gate_n} and $\overline{V_{gate\_n}}$ signals to worsen the simulation condition. Simulated waveforms of the conventional structure and proposed structure are shown in Figure 6(a) and (b), respectively. There are three gate signals. Each of the three gate signals is enabled in sequence at intervals of the line time. The concerned pixel electrode changes to the data voltage when the second gate signal is enabled. When the gate signal is disabled, the pixel electrode voltage is dropped as Equation (1). There is an additional error by the channel charges. At the proposed pixel structure, the pixel electrode voltage is compensated by the dummy switch TFT after a time of the gate delay of the inverter. The pixel voltage is not perfectly compensated by the mismatches in the parasitic

Table 1. Simulation conditions

Panel size	40”
Resolution format	1920 x 1080
Line time	15μs
V_{gate} and $\overline{V_{gate\_n}}$ range	-7V ~ 23V
V_{data} range	0V~6V (negative), 6V~12V (positive)
V_{com}	6V
Skew of V_{gate} and $\overline{V_{gate\_n}}$	100ns

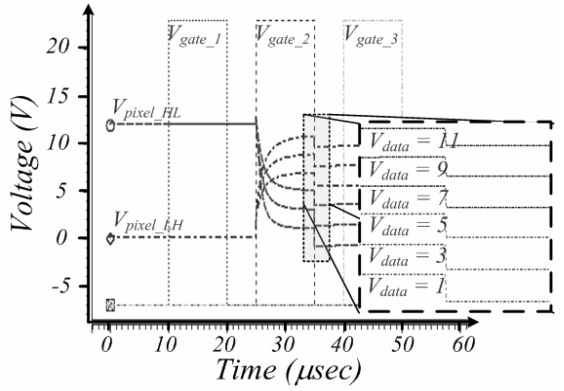
capcitances of the switch TFT and the dummy switch TFT, and the channel charge injection effect.

Simulation results of the conventional structure and proposed structure are summarized in Table 2. We simulate the ΔV_p as the data voltage by charging the pixel electrode from the 0V to the positive data and discharging it from the 12V to the negative data. In the proposed structure, the maximum value of the ΔV_p is 60mV which is compared to the maximum value of 1.82V in the case of conventional structure when the data is 1V. Because the C_{GS} is smaller than the sum of the C_{GS_dm} and C_{GD_dm}, the ΔV_p of the proposed pixel structure is positive.

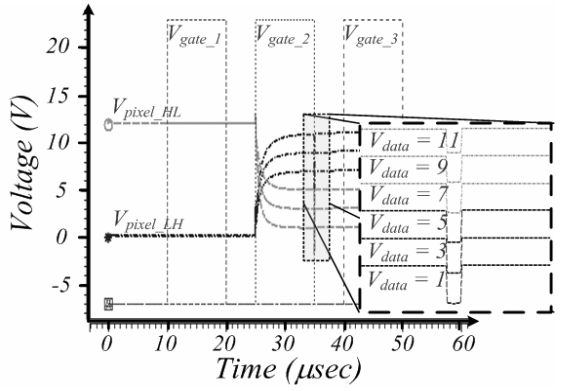
When we design the pixel, the storage capacitance, C_{STG} is determined by the leakage current of the switch TFT and the ΔV_p. As the a-Si TFT process matured, the leakage current of the switch TFT is greatly reduced. However, we can’t reduce C_{STG} because the ΔV_p is not reduced with the mature process. In the proposed pixel structure, C_{STG} can be reduced and we can secure the additional pixel area for the dummy switch TFT by reducing the ΔV_p. As a pixel layout, we can achieve the aperture ratio of 55% for the 40-in full HDTV.

5. Conclusions

In this paper, we proposed a novel technique to reduce ΔV_p by adding an additional TFT and a signal line. Then, we achieved moderate aperture ratio with simple driving method. As a result, LCD TV can be realized in high gray scale and high resolution format with a simple method.



(a)



(b)

Figure 6. Simulation results (a) conventional pixel structure, (b) proposed pixel structure.

Table 2. Simulation results

V_{data_m}	ΔV_p	
	Conventional Structure	Proposed Structure
11V	-1.16V	0.025V
9V	-1.29V	0.027V
7V	-1.42V	0.027V
5V	-1.55V	0.029V
3V	-1.69V	0.029V
1V	-1.82V	0.060V

6. References

[1] S. S. Kim, B. H. Berkeley, J. H. Park, T. Kim, and D. G. Kim, "Super PVA Achieves Ultimate LCD-TV Performance Leadership," *in Proc. of IMID,* 2005, pp. 15-20.

[2] J. H. Kim, B. D. Choi, and O. K. Kwon, "1-Billion-Color TFT-LCD TV with Full HD Format," *IEEE Trans. Consumer Electronics*, vol. 51, no. 4, Nov. 2005, pp. 1042-1050.

[3] Y. Zhu, M. Li, J. Yuan, C. Liu, B. Yang, and D. Shen, "Simulation of Pixel Voltage Error for a-Si TFT LCD Regarding the Change in LC Pixel Capacitance," *IEEE Trans. Electron Devices*, vol. 48, no. 2, Feb. 2001, pp. 218-221.

[4] K. B. Kim, S. G. Kim, O. K. Kwon, J. H. Kim, H. G. Yang, J. S. Yoo, C. B. Park, and K. W. Whang, *Display Engineering II*, Cheongbeom, Seoul, 2000.

[5] *Raphael ver. 3.3* TMA.