Active Matrix Technologies for AMLCD and AMOLED Application

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Abstract

The Chair of Display Technology at the University of Stuttgart develops various technologies for active matrix applications. Last year we presented an LTPS active matrix process without the need for ion implantation. This process is compared to other AM processes and the technological demands for different applications are discussed.

1. Introduction

Different display applications require different technologies for realizing the active matrix. Often there is a trade off between requirements, technical possibilities and production cost to determine which process is suitable and applicable for the desired display application and production.

Low temperature poly silicon (LTPS) technology is widely accepted for AMOLED displays [1]. Due to the two orders of magnitude higher carrier mobility compared to amorphous silicon (a-Si), LTPS thin film transistors (TFTs) can provide much higher current than a-Si TFTs. For this reason and because of the better device stability (eg. threshold voltage shift and output current stability) under DC operation LTPS is preferred for AMOLED application. Drawback of LTPS technology is the more complicated topgate process, the need for extra equipment for excimer laser annealing (ELA) and ion implantation and the limitation of substrate sizes. This makes the process expensive and incompatible with todays a-Si production lines. An additional advantage of LTPS compared to a-Si is the availability of CMOS technology that enables the integration of high performance driving circuitry to eliminate external drivers and to save costs for AMOLED production.

Microcrystalline silicon (µc-Si) directly deposited by plasma enhanced chemical vapor deposition (PECVD) is a promising material for cheaper active matrix display manufacturing. Bottom gate µc-Si TFTs show electron mobilites slightly higher than a-Si but are stable under DC operation [2]. This process is compatible with a-Si production lines and could be used for reducing the costs for AMOLED display production. Topgate µc-Si TFTs are more complicated to manufacture but show higher carrier mobilities than the bottomgate devices and the effort is still less than for LTPS production. In the meanwhile electron mobilities up to 150cm²/Vs are reported [3], but the devices still suffer from high leakage currents. This process might have the potential to replace LTPS in some applications.

For the application in flexible displays especially in combination with bistable display effects TFTs realized with organic semiconducting materials have gained more and more attention recently. For really flexible displays conventional inorganic TFT technologies like a-Si are not well suited because of the different thermal, mechanical and structural properties compared to plastic substrates. Active matrix displays with a-Si TFTs on plastic substrates have been realized in the past [4] but for the mentioned reasons display sizes and bendability are limited. However with organic TFTs even rollable displays have been demonstrated in the meanwhile [5].

We have developed simple and cost effective LTPS processes for active matrix display applications. The NMOS and PMOS processes were proven by manufactured display demonstrators. With the CMOS process TFTs, inverters, ring oscillators and shift registers have been realized.

For future flexible displays we are investigating alternative technologies for realizing TFTs and active matrixes on flexible substrates. Promising technologies are microcrystalline silicon for AMOLED displays and organic or carbon nanotube TFTs for LCD or electrophoretic displays based on active matrixes.

2. Results

2.1 Self aligned implanted LTPS TFT process

For AMOLED application we have developed a four mask LTPS TFT process with self aligned formation of the drain and source areas by ion implantation. The process flow is as follows:
First a buffer layer of SiO_2 and an intrinsic a-Si layer are deposited by PECVD. After dehydrogenation single area excimer laser crystallization (SAELC) [6] is performed. The semiconductor islands are defined with the first photolithography step and plasma etching. The gateoxide is deposited by PECVD and after sputter depositing the gate metal the gate electrodes are defined with the second mask step and wet chemical etching. Drain and source areas are created by self aligned ion implantation and a second excimer laser treatment for dopant activation. The interlayer dielectric, that acts as passivation as well, is deposited by PECVD and the third mask is used to define the vias that are opened by reactive ion etching (RIE). After sputter depositing the drain/source metal the fourth mask step for patterning the contacts completes the TFT process.

Average TFTs built with this process show a p-channel mobility of 40cm²/Vs, an on/off ratio of more than $5*10^6$ and a subthreshold slope of 750mV/dec.
Based on this process we have developed and realized active matrix backplanes for full color 4.4 inch qVGA OLED displays [7].

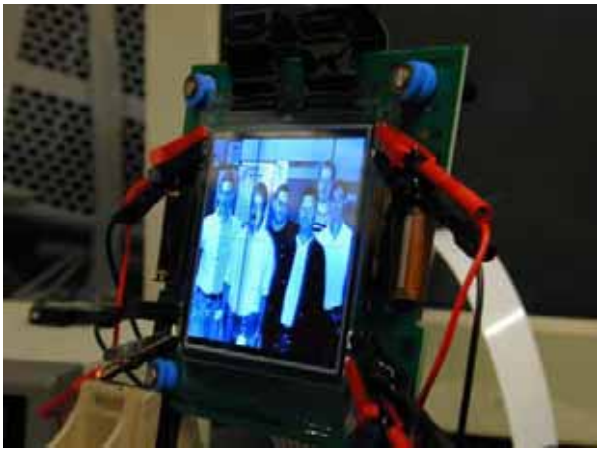


Figure 1: 4.4'' qVGA AMOLED display demonstrator (monochrome blue)

We implemented a three TFT p-mos pixel circuit which provides the possibility for testing the active matrix prior to the OLED deposition. This circuit enables additionally the measurement of OLED forward voltages at given currents to compensate for the aging during the lifetime of the display. The OLED depositions and the back end were performed by project partners within the OLEDFAB consortium [7]. A photograph of one of the realized demonstrators is shown in Figure 1. The distorted columns in the left part of the display are caused by failed bond contacts of one of the column drivers.

2.2 LTPS TFT process with deposited drain/source areas

The self aligned implanted 4 mask LTPS TFT process works well for p-channel TFTs where no low doped drain (LDD) is required. Implementing additional LDD structures for improved n-channel operation increases the number of implantation steps and, dependent on the process, even the number of required masks [8]. This is raising the production costs considerably. Furthermore ion implantation equipment is among the most costly equipment for LTPS backplane manufacturing and a limiting factor for substrate sizes. For these reasons we have developed an LTPS active matrix process with PECVD doped drain/source contacts [9]. The implantation free low temperature poly silicon TFT process is illustrated in Figure 2. A PECVD deposited layer is used as dopant source. The substitution of ion doping by PECVD deposition overcomes a major limitation for panel sizes in poly-Si technology and avoids large investment costs for ion implantation equipment.

First a highly doped silicon layer is deposited by PECVD. The doped silicon is structured by photolithography and plasma etching to form the drain and source region of the TFT in a later process step (a). After that the intrinsic silicon layer is deposited (b). The two PECVD processes were adapted to each other, in order not to incorporate the phosphorous to the TFT channel by etchback of the doped silicon during the deposition of the intrinsic silicon. After dehydrogenation the amorphous silicon is crystallized with an area excimer laser and is structured to islands (c). Within the laser crystallization step the dopant atoms diffuse to the

overlaying silicon, are activated and form the drain and source region.
After PECVD deposition of the gateoxide the gate metallization is sputter deposited and structured wet chemically (d). Because of the non self aligned process the gate has to overlap drain and source to avoid an offset region by misalignment during the photolithography.
To complete the TFTs, the interlayer dielectric is deposited (e), via holes are opened and the contact metallization is sputter deposited and structured (f).

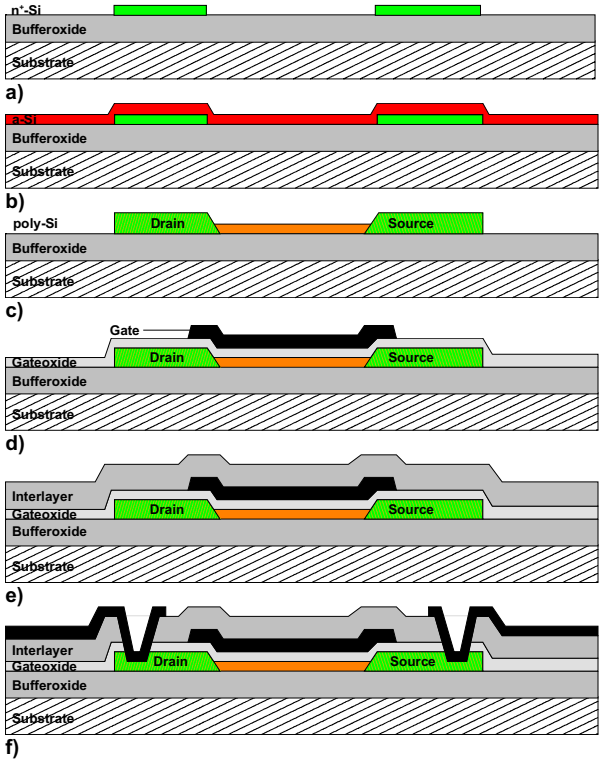


Figure 2: Process flow for poly-Si TFTs with PECVD doped drain/source areas

With this process we were able to fabricate operating TFTs over a 120mJ/cm² wide range of laser energy densities. The process allows the fabrication of TFTs with different electron mobilities for active matrix and driving electronics integration on the same panel. Dependent on the applied laser energy density TFTs with electron mobilities of μ_e=20cm²/Vs (at 520mJ/cm²) up to μ_e=200cm²/Vs (at 640mJ/cm²) were processed on the same glass substrate (see Figure 3). The in situ dopant diffusion and activation during the laser crystallization forms a self aligned gate overlapped LDD [10] without any additional process step. Implant damage at drain/source junctions which is difficult to anneal completely in a self aligned implanted TFT process [11] is avoided as well.

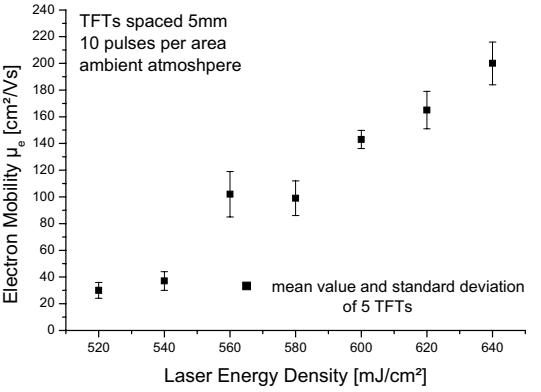


Figure 3: Electron mobility versus laser energy density

For application as switching TFTs in AMLCD or AMOLED displays we realized TFTs with a channel geometry of 20µm*20µm with and without doped region in the channel. The selectively doped region (SDR) reduces the off-current by lowering the electrical field at the drain junction in the off-state without reducing the drain current in the on-state [12]. With this method we realized TFTs with an electron mobility of μ_e=200cm²/Vs and an on/off ratio > 10^7. Input characteristics of TFTs with/without SDR are shown in Figure 4.

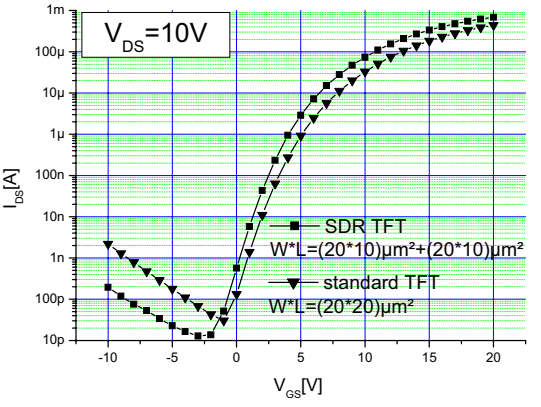


Figure 4: Input characteristic of TFTs with/without SDR

For application in AMOLED displays additionally to switching TFTs current driving TFTs are required. These TFTs require good saturation to compensate for aging of the OLEDs [13] (the luminance/current

characteristic of the OLED is less changed during aging than the I/V characteristic). For this purpose we realized TFTs with a channel geometry of W*L=10µm*40µm. These TFTs show an excellent saturation compared to TFTs with a channel geometry of W*L=20µm*20µm as depicted in Figure 5.

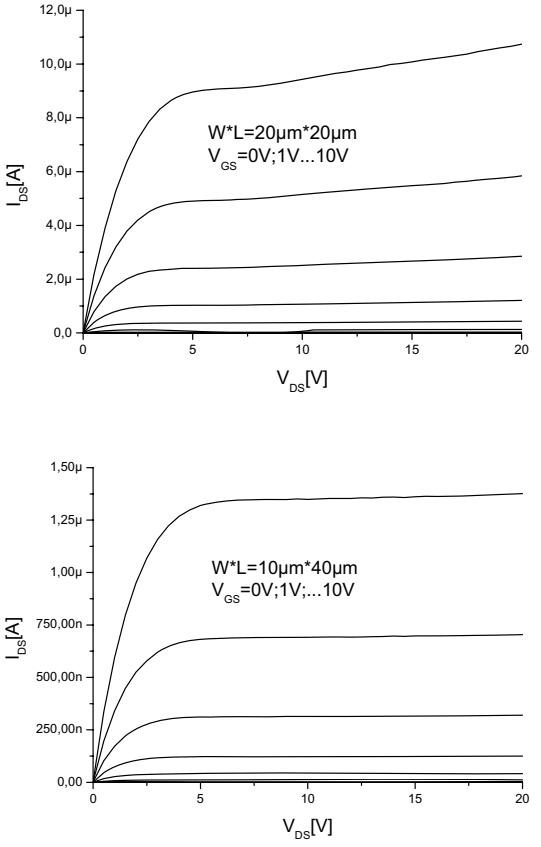


Figure 5: Output characteristics of TFTs with different W/L ratio

To verify the process described here we have realized a 4-inch full color quarter-VGA poly-Si AMLCD. The active area of the display is 80mm*60mm, with a subpixel pitch of 83µm*250µm. The display was addressed with a dedicated addressing system with a Field Programmable Gate Array (FPGA) as its core that was developed in our lab [14],[15]. The complete display (including photolithographic masks, Active Matrix backplane and color filter/black matrix frontplane) were developed and manufactured at the Chair of Display Technology. The full color AMLCD addressed with display drivers and dedicated addressing system is shown in Figure 6. The column errors concentrated in one part of the display are caused by misaligned bond contacts of the driver TCP to the columns of the matrix, resulting from the 52µm column driver pitch which was difficult to handle with our actual (self built) bonding tool.

Figure 6: full color 4'' quarter VGA AMLCD addressed with display drivers and dedicated addressing system

This process allows for the realization of large size LTPS active matrixes without the size limitation and investment cost for ion implantation equipment.
Based on this process we are working on the development and implementation of an AMOLED display with integrated parts of the addressing circuitry.

2.3 Five mask CMOS LTPS process with LDD and only one ion implantation step

To reduce the number of masks steps required for the production of CMOS LTPS backplanes with integrated driver electronics we have developed a five mask CMOS process with LDD and only one ion implantation step as a combination of the processes presented in the sections 2.1 and 2.3 of this paper [16]. The drain and source areas for the n-channel TFTs are deposited by PECVD and patterned subsequently. The intrinsic a-Si for all channel areas is deposited in one PECVD step. After excimer laser crystallization, gate oxide deposition and patterning of the gates self aligned ion implantation forms the drain/source areas for the p-channel TFTs. For the detailed process and results see ref. [16]. The TFT properties manufactured with this CMOS process are comparable to characteristics of the TFTs

manufactured with the PMOS and NMOS processes presented in section 2.1 and 2.2. Till now we have realized single TFTs, inverters, ring oscillators and shift registers with this process.
The simple and cost effective five mask CMOS process enables the realization of large area (for example n-type) active matrices with high performance CMOS driver electronics at the borders of the matrices. With an appropriate moving stage ion implantation can be performed without the need for having line beam ion sources as wide as the substrates which could improve throughput and lower equipment cost.

2.4 a-Si and µc-Si TFT processes

Another possibility to reduce the costs for AMOLED display production could be the utilization of a-Si or µc-Si TFTs for this application. Amorphous silicon technology still suffers from the device instability under DC operation. It is not yet ready for being commercialized in AMOLED display production [1]. But the implementation of bottomgate TFTs with PECVD deposited µc-Si promises stable devices with an a-Si production line compatible process. Stable TFTs under DC-operation with electron mobilities up to 3cm²/Vs have been reported [2].

In the past we have developed a-Si TFT active matrix displays for various applications among them high resolution LCDs with high aperture or an AMLCD on plastic substrate [17],[4]. Our actual task of research in this area is the implementation and optimization of a bottomgate µc-Si TFT process on steel foil. By adopting and optimizing the PECVD silicon deposition process we were able to achieve a crystallinity of the active layer at the interface to the gate dielectric of 80% within the whole substrate area of 14''x14''. The results from first realized TFTs are promising. The device properties are stable under dc operation but suffer from a too low on/off ratio of 10^4 at the moment. The optimization of the process is ongoing.

2.5 Alternative TFT technologies for flexible display applications

TFTs with organic semiconducting materials for the channel layer have big potential for flexible display technologies. These organic TFTs (OTFTs) are suitable for a wide range of applications where flexible substrates or low cost circuitry are required. The thermal, structural and mechanical properties of organic semiconductors are well adapted to those of flexible plastic substrates.

For flexible active matrix displays especially in combination with bistable display effects TFTs realized with organic semiconducting materials have gained more and more attention recently. Even rollable displays have been demonstrated in the meanwhile [5]. Different deposition methods like spincoating or different printing technologies up to roll-to-roll processes and a big variety of organic semiconductors are under research at the moment [18],[19]. Higher carrier mobilities can be achieved by using evaporated organic semiconductors or by increasing the molecular order with especially designed polymer materials [20].

We have developed an OTFT process on plastic substrates using evaporated pentacene as semiconductor and a gatedielectric prepared by anodic oxidation of the gatemetalization [21]. The anodic oxidation of the gatemetal provides a high quality gatedielectric formation at room temperature. The electrical performance of this oxide is exceptionally good, even for thin layers. TFTs realized with this method show a high on/off ratio at low operation voltages. Figure 7 shows the input characteristic of a bottom gate, bottom contact pentacene TFT with Al_2O_3 as gate dielectric manufactured on PES foil.

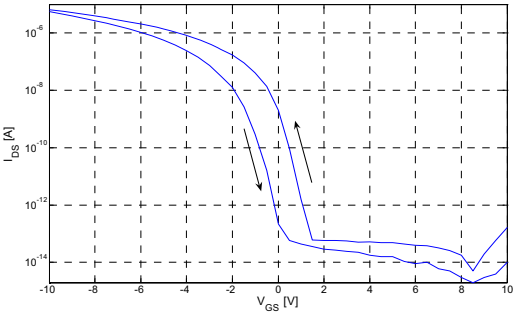


Figure 7: Input characteristic of pentacene TFT on PES foil measured forward and reverse

An on/off ratio of 10^8 is achieved with -10V gate and -10V DS voltage. This is about 2 orders of magnitude higher than with a-Si TFTs manufactured on PES foil [4]. The hole mobility of 0.1cm²/Vs is comparable to the electron mobility of the a-Si process on PES foil. The reason for the hysteresis is under investigation. It is not only related to the gatedielectric process. With

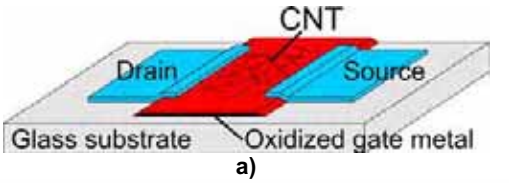
PECVD SiO_2 we observe even higher hysteresis. First experiments indicate an influence of present humidity on surfaces and ambient on the hysteresis behavior.

Based on this OTFT process we are working on the realization of flexible active matrix displays. Encapsulation of the OTFT on plastic foil still is a challenging task.

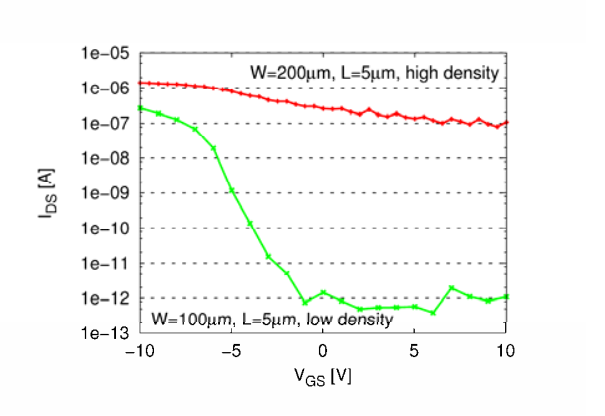
Another new, promising technology for realizing displays on flexible substrates are carbon nanotube (CNT) layers. In a display there are two possible applications for CNT layers. Nanotube layers can act as transparent conductive layers to replace ITO [22] or as semiconductor layer in TFTs [23],[24].

We have investigated both possibilities [25]. For both applications (conducting layer and TFT channel) we utilized CNT networks. The carbon nanotube networks were deposited from dispersion in surfactant solution at substrate temperatures of 80°C or even at room temperature. For gate and gate dielectric we used the same process than for our OTFTs. Figure 8a) shows the schematic of the realized CNT TFTs. The processes are completely compatible with plastic foil substrates.

For transparent conductive layers so far we have reached a resistance of 400 ohms/square at a transmission of 80% in the visible range. The input characteristics of TFTs with different CNT densities in the channel area are shown in Figure 8b). The differences in the device behavior are caused by the fact that from the nature of the structure of the tubes the CNTs exist in a mixture of approximately 1/3 metallic CNTs and 2/3 semiconducting CNTs. So far there is no possibility to separate the conducting from the semiconducting tubes in a technically applicable process. Our TFT production is based on the theory of lowering the density of the CNT network to a point where single current paths through the network are formed between drain and source of the TFT with at least one semiconducting nanotube in each path. The high density network shows almost metallic properties. By reducing the nanotube concentration the semiconducting properties get more and more visible. The realized TFTs show device mobilities of up to 1cm²/Vs and an on/off ratio of 10^5. The real carrier mobility is much higher. For the calculation we used the standard MOSFET equation not taking into account that the current is only flowing in single paths through the network and not homogeneously over the complete channel width.



a)



b)

Figure 8: CNT TFT a) schematic b) input characteristic

Big challenge at the moment is to improve the homogeneity and reproducibility of the process. For the carbon nanotube technology there is still a long way of development to go before it can be implemented in displays, but the results achieved are very encouraging to go on with this work.

3. Conclusion

Reducing the cost for AMOLED backplane production and developing new active matrix technologies for novel flexible display applications are two of the big challenges in today's display research. We have developed an AMOLED capable 4-mask LTPS process with self aligned ion implantation and an LTPS process with PECVD doped drain/source areas that does not require ion implantation any more. These processes have been proven by realization of AMLCD and AMOLED display demonstrators. As a combination and enhancement of both processes we have developed a 5-mask CMOS LTPS process with LDD and only one ion implantation step. Furthermore we have presented our latest results in developing organic and carbon nanotube TFTs for application in future flexible active matrix displays.

4. Acknowledgements

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