Bias stress effect in organic thin-film transistors with cross-linked PVA gate dielectric and its reduction method using SiO_2 blocking layer

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Abstract

Bias stress effect in pentacene organic thin-flim transistors with cross-linked PVA gate dielectric is analyzed. For negative gate bias stress, positive threshold voltage shift is observed. The injected charges from the gate electrode to the defect states of gate dielectric are regarded as the main origin of V_T *shift. The reduced bias stress effect using* SiO_2 *blocking layer confirms the assumed mechanism. It is also demonstrated that the inverter with* SiO_2 *blocking layer shows the negligible hysteresis owing to the reduced bias stress effect.*

1. Introduction

The research of bias stress effect in organic thin-film transistors (OTFTs) is very important for the reliable operation of organic circuits. In organic electronics such as radio-frequency ID transponders, smart tags, and flexible integrated electronics [1-3], the threshold voltage shift caused by bias stress might bring about unexpected operation. Therefore, to reduce the bias stress effect, the research of its mechanism is necessary.

Among various organic gate dielectrics, cross-linked poly vinyl alcohol (PVA) is one of the promising materials because it has a high dielectric constant [4], photosensitivity [5], and fine immunity to solvents involved in the lift-off process. However, relatively large hysteresis due to the bias stress in the OTFTs with cross-linked PVA has been a serious problem [6].

In this paper, bias stress effect in pentacene OTFTs with cross-linked PVA gate dielectric is studied. From the analysis of bias stress effect, a stress reduction method using SiO_2 blocking layer is proposed. To investigate the circuit operation of the proposed device, an inverter consisting of an enhancement mode driver and a load is implemented.

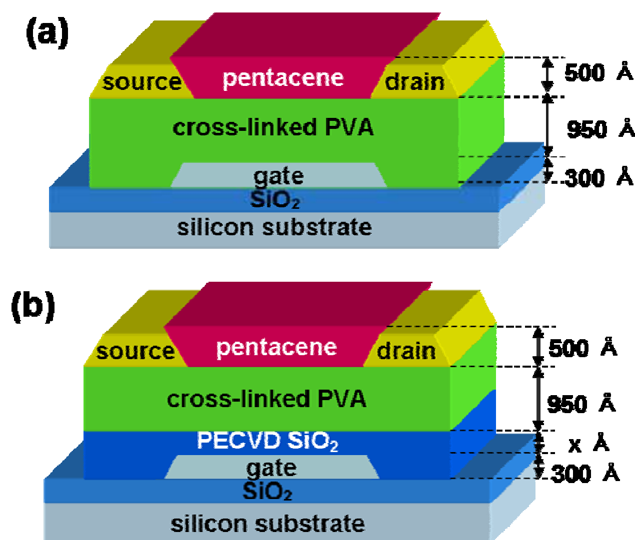

Figure 1. Structure of bottom-contact OTFT. For the contrastive analysis, two types of gate dielectric are fabricated: (a) cross-linked PVA monolayer, and (b) PECVD SiO_2/cross-linked PVA bilayer

2. Experiment

Figure 1 shows the structure of the fabricated bottom-contact OTFT on oxidized silicon substrate. The titanium (Ti) gate electrode is evaporated and patterned by photolithography and wet etch.

For the organic gate dielectric, 2 % PVA solution mixed with ammonium dichromate photo-sensitizer is spin-coated and patterned by UV exposure [1]. To demonstrate the effect of charge blocking layer, the OTFT with plasma enhanced CVD (PECVD) SiO_2/cross-linked PVA gate dielectric is also

fabricated. The gold (Au) source/drain (S/D) formation is carried out by photolithography and lift-off process. The device is completed using thermal evaporation of pentacene at high vacuum ambient of around 10^{-8} Torr. The substrate temperature is 80 ℃, and the active region is patterned by a shadow mask.

To investigate the bias stress effect, negative gate bias of -10 V is applied to both devices. The device characteristic is quickly measured and the bias stress immediately resumed. The drain voltage is fix ed to -0.1 V to minimize the effect of drain bias during the characteristic measurement. The characteristics of the devices are measured with a probe station and semiconductor parameter analyzer Agilent Technologies 4156C in a light-shielded environment.

3. Results & Analysis

Figure 2 illustrates the transfer characteristics of OTFT with cross-linked PVA gate dielectric during the negative gate bias stress and after relaxation. It is shown that the main effects of the stress are positive threshold voltage (V_T) shift and the degradation of subthreshold swing. However, the field-effect mobility does not change significantly during the measurement.

Possible mechanisms responsible for the positive V_T shift include electron injection into the gate dielectric, polarization effect, and mobile ion movement in the gate dielectric. However, the large positive V_T shift and the time-dependent V_T shift hardly be caused by polarization or mobile ion effect in the cross-linked PVA. These observations could suggest that the mechanism of the V_T shift may be charge (electron) injection from the gate electrode into the gate dielectric. The injected electrons are trapped in the electron trap states, thus hole accumulation in the channel is enhanced. Accordingly, the OTFT turns on more rapidly and the on current increases during the stress time.

In addition, it is observed that the measured threshold voltage after relaxation is similar to the initial value. The complete relaxation is observed about 1 day later, but most V_T recovery is showed after a few hours. The reversible characteristic implies that most injected charges are trapped in the shallow defect states in cross-linked PVA gate dielectric.

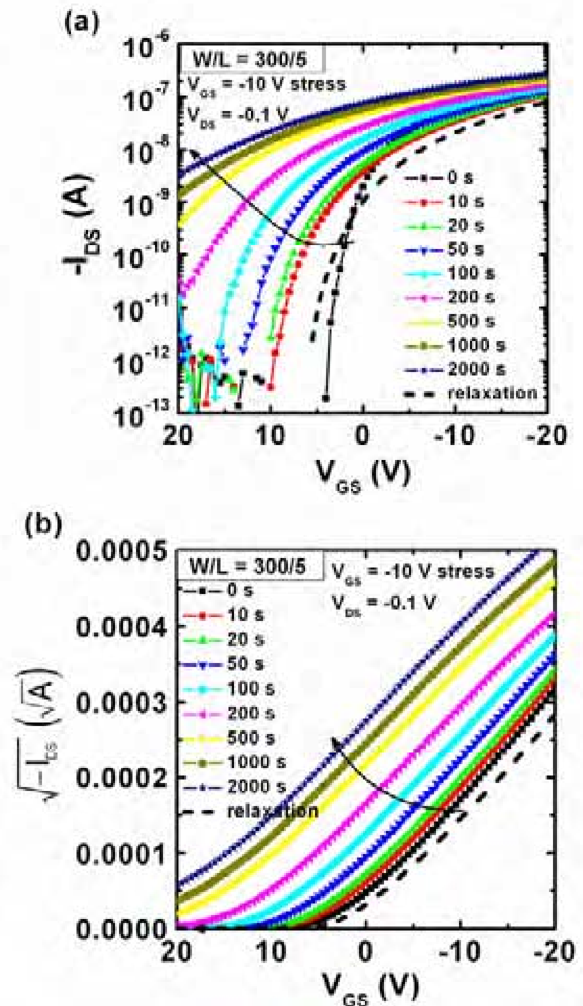

Figure 2. Transfer characteristics of the OTFT with cross-linked PVA during the negative gate bias stress and after relaxation. (a) $-I_{DS}$ in log scale (b) $\sqrt{-I_{DS}}$ in linear scale

Figure 3 shows the reduced bias stress effect in transfer characteristic using PECVD SiO_2 blocking layer. The structure of the device is shown in figure 1(b). In this device structure, considerably reduced positive V_T shift is obtained. Instead, a negative V_T shift stress is observed after 200 second bias stress. This phenomenon verifies the charge blocking effect of the SiO_2 layer in the gate dielectric. In this case, the holes are injected from the pentacene and then, trapped in the defect states of cross-linked PVA/pentacene interface. This mechanism is considered as the main origin of the negative V_T shift.

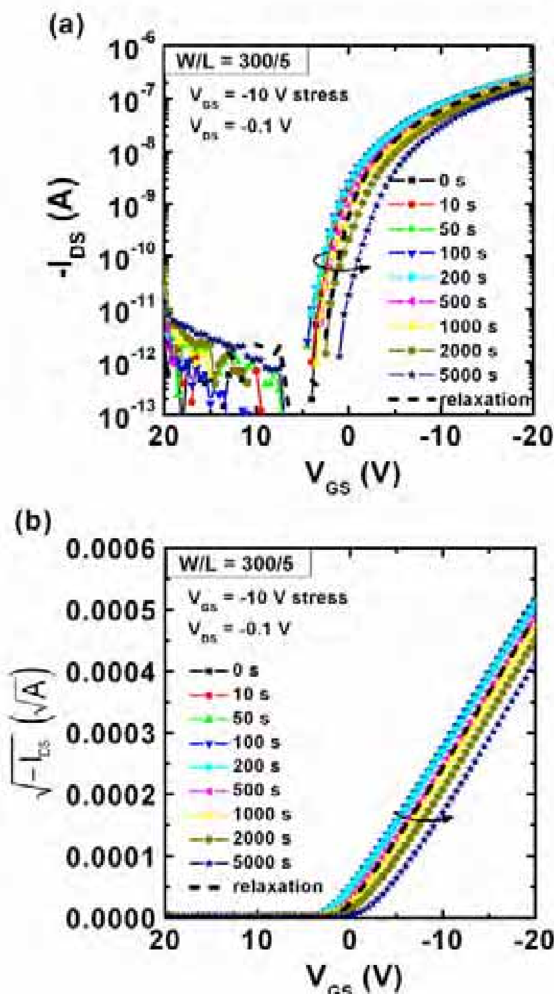

Figure 3. Transfer characteristics of the OTFT with PECVD SiO_2/cross-linked PVA during the negative gate bias stress and after relaxation.

(a) $-I_{DS}$ in log scale (b) $\sqrt{-I_{DS}}$ in linear scale

The recovered V_T after relaxation clarifies the existence of shallow defect states as in the previous case. However, the recovered V_T is not the same as initial V_T. So, we can not eliminate the existence of deep trap states.

The threshold voltage shift (ΔV_T) as a function of time are depicted in figure 4 for both devices. Using the PECVD SiO_2 blocking layer, the abnormal increase of threshold voltage after the bias stress is effectively reduced. Moreover, there is almost no V_T shift until 200 second bias stress. This phenomenon might support the application of proposed device in the RFID transponder circuit which is operated for relatively short time.

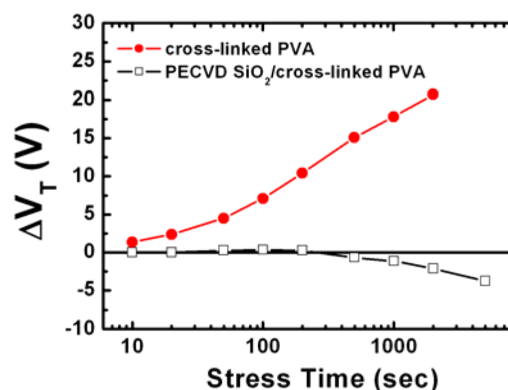

Figure 4. Threshold voltage shift (ΔV_T) as a function of time. Considerably reduced ΔV_T is observed using PECVD SiO_2 blocking layer.

4. Organic Inverter

Figure 5 illustrates the schematic diagram of the integrated inverter and the voltage transfer curves (VTC). The inverter consists of an enhancement mode driver and a enhancement load. In this measurement, the input voltage is swept both forward and backward to investigate the hysteresis characteristic. As shown in the figure, the hysteresis is very small so that, the reliable operations of the organic circuits is expected. The negligible hysteresis is caused by the reduced bias stress effect using the SiO_2 blocking layer. Based on the results, the use of SiO_2 blocking layer can be suggested as a possible solution to the hysteresis problem that many organic devices are facing with.

5. Conclusions

Bias stress effect and its mechanism in OTFTs with cross-linked PVA gate dielectric are analyzed and investigated. Moreover, a novel method to suppress the bias stress effect is proposed and the effect is demonstrated for the first time. It is also demonstrated that the inverter with SiO_2 blocking layer shows the negligible hysteresis owing to the reduced bias stress effect. The proposed hybrid gate dielectric will bring about reliable operations of the organic circuits.

6. Acknowledgements

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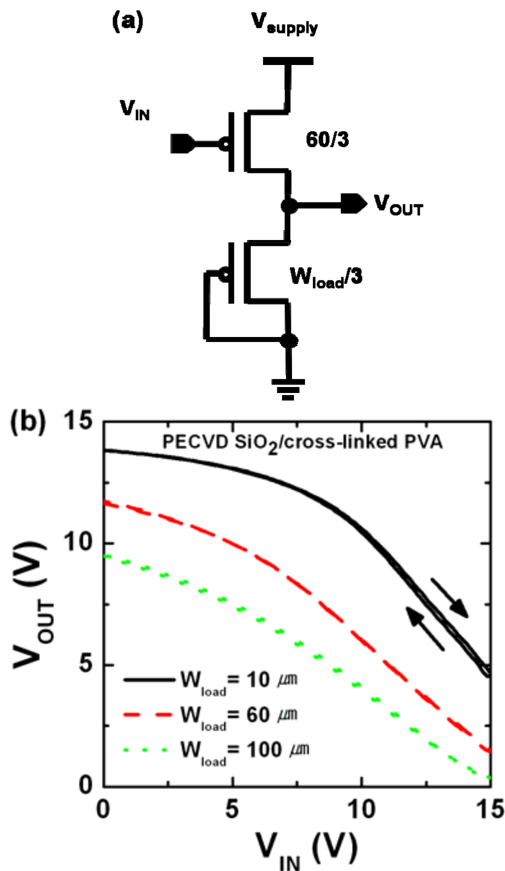

Figure 5. (a) Schematic diagram of the inverter (b) Voltage transfer curves for PECVD SiO_2/cross-linked PVA gate dielectric.

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