Near 100°C low temperature a-Si TFT array fabrication on 7 inch flexible PES substrates

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Abstract

High-quality a-Si TFTs were fabricated on 7 inch plastic PES substrates at 130°C and 100°C. It had been shown that the key factor for successful TFT fabrication on the relatively large plastic substrates is thorough control of total active layer's stress by means of deposition temperature reduction and single layer's intrinsic stress optimization.

1. Introduction

Thin film transistor **(TFT)** fabrication on flexible plastic substrates attracts increased attention due to the need for light, foldable and unbreakable displays. The major issue of plastic integration is incapability of most of the plastic substrates to withstand high temperatures, so, conventional (~370°C) a-Si TFT manufacturing process is impossible on the plastic.

Until now several research attempts were focused on the development of low temperature a-Si TFT fabrication and materials optimization at various temperatures from 75°C to 150°C **[1-7]**. Some authors achieved really impressive TFT performance on the glass i.e. mobility up to 0.75 cm^2/Vs at 150°C **[6]**, 0.8 cm^2/Vs at 120°C **[5]** or 0.38 cm^2/Vs at 75°C **[7]**. The highest mobility achieved on the plastic (Kapton HN substrates) is 0.4 cm^2/Vs **[4]** and 0.8 cm^2/Vs **[5]** at 120°C. At the same time, despite relatively low coefficient of thermal expansion (CTE), providing lower thermal stress of the active layer and less layer-to layer misalignment, Kapton substrates have amber color and can't be used for high-quality color displays. Also, some applied process parameters (low deposition rates for example) are probably not consistent with mass production requirements.

Most publications on plastic TFT do not pay sufficient attention to the problem of plastic substrate size and large area deposition. In our work on plastic TFT fabrication on PES substrates we encountered the problem of active layer lifting when active layer's stress was too high and this problem becomes more severe when the plastic substrate size increases. So, in contrast to TFT fabrication on the glass, there are strict limitations for the total active layer's stress on the plastic and exceeding of a certain limit leads to active layer lifting. Taking this into account the main goals of the present work were:

1. To reduce the total active layer's stress by means of low temperature deposition and single layers' intrinsic stresses reduction.
2. To improve TFT performance at 130°C and 100°C by single layers optimization, while keeping active layer's stress below the "lifting-free" limit.

1.1. Experimental

In this study we started from "standard" CVD recipe, chosen from previous experiments. To analyze single layers' properties all studied films (SiN_x, a-Si, n^+-Si) were deposited by 13.56 MHz PECVD at 130°C and 100°C on <100> oriented silicon wafers. SiN_x films were deposited from $SiH_4/NH_3/H_2$ mixture; to enhance the layers' quality H_2 dilution was applied for SiNx, a-Si and n^+-Si deposition.

Thicknesses of corresponding layers were measured by ellipsometry (FPD-100, J.A. Woollam Co., Inc.). Stress measurements were conducted at room temperature using "FSM-500TC" temperature controlled film stress measurement system. Inaccuracies of films' thicknesses can be caused by ellipsometry data fitting errors and by films' thicknesses non-uniformity across the wafer. Overall these inaccuracies were estimated to be within the limit of 0.5-1%. Inaccuracies in total stress calculation, estimated to be less than 5% are due to the film's thickness uncertainty, variation in wafer position inside the measurement chamber and some variation of films' properties. The total stress of active layer deposited on the silicon wafer was calculated as a sum of each single layer's (SiN_x, a-Si, n^+-Si) stress multiplied by the layer's thickness and divided by the total active layer's thickness.

Finally, inverted staggered, back-channel etched a-Si TFT arrays were fabricated on 30×40 cm glass and 7 inch PES plastic substrates, attached to the carrier glass by means of special adhesive material. Some details of plastic substrate handling and TFT fabrication process can be found in **[8]**.

TFT performance was measured in 5 different points, located in the center and on the edges of the plastic substrate or glass. Each measured "TEG" comprises 100 TFTs connected in series. We observed some dispersion in TFT performance, measured on different "TEGs", that is due to non-uniformity of layers' thicknesses and dry-etch non-uniformity. TFT transfer curves were measured at Vsd=10V and Vgs sweep from -20V to +20V. TFT mobility was measured using Vgs=Vsd sweep from -3V to +20V and TFT Vth values were calculated in the linear region of the curve from ~15V to +20V.

2. Results

In contrast to the previous study (at 150°C), in the present work we switched to 130°C and 100°C PECVD, as far as lower deposition temperature provides the following advantages:

1. Less bending of the carrier glass due to less irreversible dimensions' changes of the plastic substrate after "high-temperature" process steps
2. Lower layer-to-layer misalignment after patterning
3. Significant reduction of the active layer's stress

Other things being equal (deposition temperature, substrate, active recipe), the next step to reduce total active stress is to reduce intrinsic stress component, which depends on the PECVD deposition conditions (at fixed temperature). It was demonstrated that SiN_x films, deposited at lower plasma power possess much lower intrinsic stress. In contrast to SiN_x film behavior, stress vs. temperature dependence is not so abrupt for a-Si films: plasma power decrease results only in a little higher film stress (stress is becoming more compressive, **Figure. 1)**.

It appeared that SiN_x film's stress can be varied in a large range by means of plasma power variation. Using these SiN_x films a number of active recipes with different intrinsic stresses (from -5.33×10^9 to -2.34×10^9 dyne/cm^2) were prepared and tested on 7 inch PES substrates in order to find out the "lifting-free" limit of the intrinsic active stress ("lifting-free" limit is defined as the stress value when the frequency of lifting occurrence is less than 10%). In case of our 7" PES plastics this limit was found to be ~ -3.30×10^9 dyne/cm^2 (total active layer thickness 6000Å) at 130°C active deposition, nevertheless this value is supposed to be dependant on the plastic substrate handling history (moisture content, annealing temperature and time, type of adhesive material), so, in each particular case "lifting-free" limit should be identified independently.

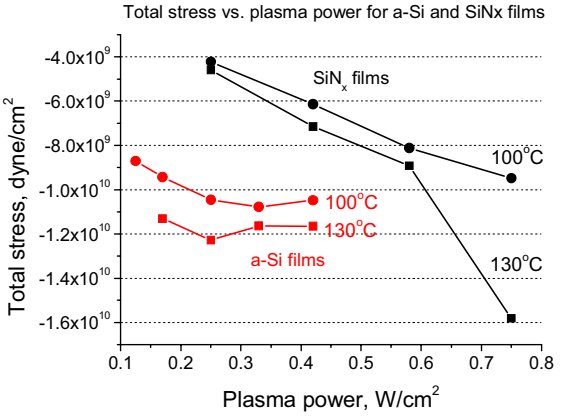

Figure. 1 Total stress vs. plasma power dependence for a-Si and SiN_x films (130, 100°C)

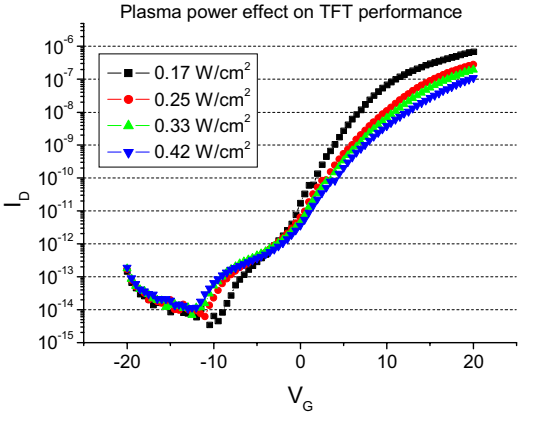

Figure. 2 Plasma power effect on TFT performance at 100°C

In the course of TFT performance improvement it was found out that lower plasma power, applied for a-Si deposition, resulted in notably higher TFT mobility and on-current values **(Figure. 2)**. At the same time reduction of plasma power of SiN_x deposition led to *slight* TFT performance deterioration. That is why in order to reduce active layer stress, while keeping the best TFT performance we applied the lowest stress

SiN_x layer and the best quality a-Si layer, both deposited at low plasma power.

Deposition at lower plasma power results in higher [SiH/SiH2] ratio of a-Si film providing lower defect concentration that, in turn, leads to better TFT performance **[9, 10]**. In general, the plasma power should be just high enough to provide necessary precursor activation, nevertheless it shouldn't be too high to avoid additional defect formation due to film damage by plasma species **[11]**. The same effect (increase of monohydrate bonding) is achieved by considerable H2 dilution of silane during a-Si deposition: hydrogen etches weak [SiH2] bonds thus improving [SiH/SiH2] ratio in the film **[11]**.

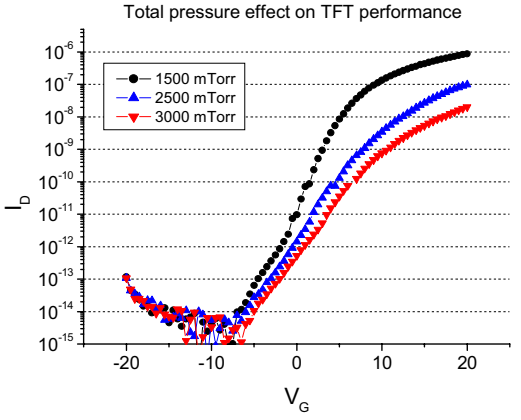

Figure. 3 Total pressure effect on TFT performance at 100°C

In addition, effect of total pressure of a-Si deposition was analyzed **(Figure. 3)**: decreasing the total pressure results in notable TFT performance improvement as far as it leads to lower a-Si deposition rate and facilitates surface diffusion resulting in better a-Si film quality.

Optimized process conditions integration resulted in the following "champion" TFT performance on 7 inch PES substrates at 130°C: μ~0.5 cm^2/Vs, I_{on}~1.1 μA, I_{off} ~3×10^{-14}A, I_{on}/I_{off} ~3×10^7, Vth~4.5V. At the same time reduction of the active layer deposition temperature to 100°C resulted in noticeable TFT performance deterioration: the highest achieved mobility and I_{on} is 0.15 cm^2/Vs and 0.2 μA, the lowest Vth is 8V **(Figure. 4)**. Such a deterioration was attributed mostly to considerable increase of S/D-(n^+-Si)-a-Si-(n^+-Si)-S/D contact resistance (CR), caused by deposition temperature reduction and resulting in much lower TFT Ion, mobility and higher Vth. In order to reduce CR "post-treatment" process was introduced to the TFT fabrication process. It was demonstrated that "post treatment" allows reducing CR thus leading to higher TFT Ion and mobility, as well as to lower Vth of "100°C TFTs" **(Figure. 4)**. The "champion" TFT performance achieved at 100°C after "post-treatment" is: μ~0.5 cm^2/Vs, I_{on}~1.2 μA, I_{off} ~1×10^{-13}A, I_{on}/I_{off} ~1×10^7, Vth~6.8V.

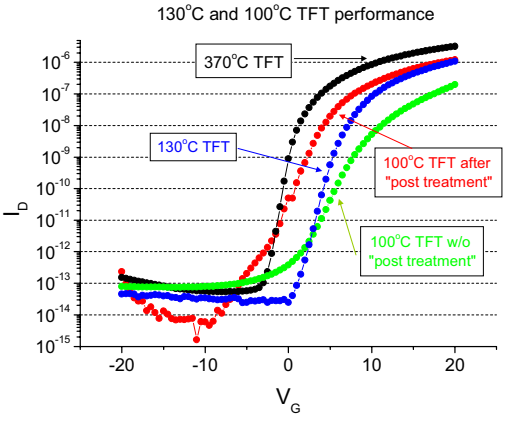

Figure. 4 Performance of "130°C TFTs" and "100°C TFTs" before and after "post-treatment"

Finally, 130°C and "100°C TFT" stability was measured using constant voltage (V_G=20V, V_{SD}=10V) TFT stress of different durations. After each stress step TFT transfer measurements were conducted according to the described above procedure. It had been shown that TFT stability somewhat deteriorates with decrease of active layer deposition temperature from 130°C to 100°C.

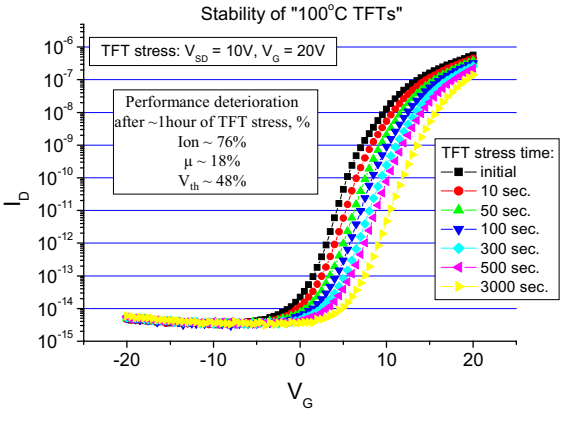

Figure. 5 Stability of "100°C TFTs"

Stability deterioration manifests itself mostly in bigger Vth shift and Ion decrease, while mobility drop is not that severe compared and no Ioff degradation had been observed even after quite long TFT stress time **(Figure. 5)**.

Surely, for successful application of "100°C TFTs" their stability should be improved and be compared to that of the "high-temperature" ones. Some possible ways to improve TFT stability are: SiNx composition modification **[12]**, proper plasma treatment of dielectric/a-Si interface **[13]**, SiNx/SiO2 double layer application **[14]** etc. Currently, for "100°C TFTs" none of TFT performance parameters (needed for successful LCD driving: Ion, μ, Ion/off) could be "sacrificed" in the course of TFT stability enhancement.

3. Conclusion

In contrast to the previous research attempts in the present work we demonstrated the ability of high-quality a-Si TFT fabrication at low temperature (130°C, 100°C). It has been shown that the key factor for successful TFT fabrication on the relatively large plastic substrates is thorough control of overall TFT stress by deposition temperature reduction and single layer intrinsic stress optimization.

We improved active layer deposition conditions for the better TFT performance and quantified relationships between TFT performance and plasma power and total pressure of a-Si film deposition. We came to conclusion that high contact resistance, caused by insufficient dopant activation in n^+-Si film is one of the main reasons for inferior performance of "low-temperature" TFTs compared to their "high-temperature" counterparts. At the same we introduced the "post-treatment" process that allows partial CR reducing that results in higher TFT Ion and mobility.

Finally, it was demonstrated that TFT stability deteriorates with decrease of active layer deposition temperature from 130°C and 100°C.

Using fabricated plastic TFTs we succeeded in driving of 7 inch 114ppi plastic LCD working sample **(Figure. 6)**.

Figure. 6 Prototype of 7" transmissive plastic TFT-LCD

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