A Low-Power and High-Accuracy Driving Method for LTPS TFT-LCD in Mobile Applications

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Abstract

A high data accuracy and low power consumption driving method and output stage of the source driver are proposed for the LTPS TFT-LCD in mobile applications. The proposed driving method is insensitive to the variations of the electrical characteristics of TFTs, which enables the output errors of the source driver are under 1/2 LSB in all gray levels. In addition, the power consumption of the driver with the method is decreased to 9.9mW which is 55.9% of that of the conventional source driver by reducing unnecessary charge waste.

1. Introduction

In a low temperature polycrystalline silicon (LTPS) thin film transistors (TFT) liquid crystal display (LCD) panel, simple analog buffers are used such as source-follower in most case because threshold voltage and mobility of LPTS TFTs are not uniform[1], [2], and thus the number of TFTs must be minimized.

Figure 1 shows the conventional output stage of the source driver using LTPS TFTs on the glass substrate for LCD. The output buffers of the source driver are used to charge the column line load in a line time. The driving method of the structure wastes more power than necessary because it doesn't have enough discharging path, thus it discharges most of the previously charged voltage in the column line through the reset TFT.

Lately, a new driving scheme has been reported to decrease the power consumption[3]. It uses two operational amplifiers per channel: one for charging and the other for discharging operation. However, this architecture increases the layout area of the output stage because of an extra operational amplifier.

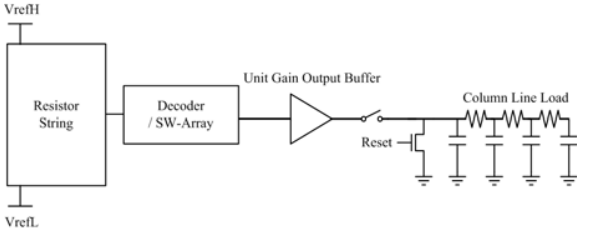

Figure 1. Block diagram of conventional source driver.

We introduce a new low-power and high-accuracy driving method without increment of the layout area.

2. Proposed Driving Method

The proposed driving method takes advantage of the difference between charging and discharging time. In general, the RC delay when charging and discharging must be same, but in the case of the DAC, there is varying on-resistance (R_{ON}) although the same size of TFTs is used. Thus the RC delays when charging and discharging are different. Figure 2(a) shows the current path between the reference voltage and the column line, and the TFTs in the switch-array of the DAC whose on-resistance dominates the load resistance

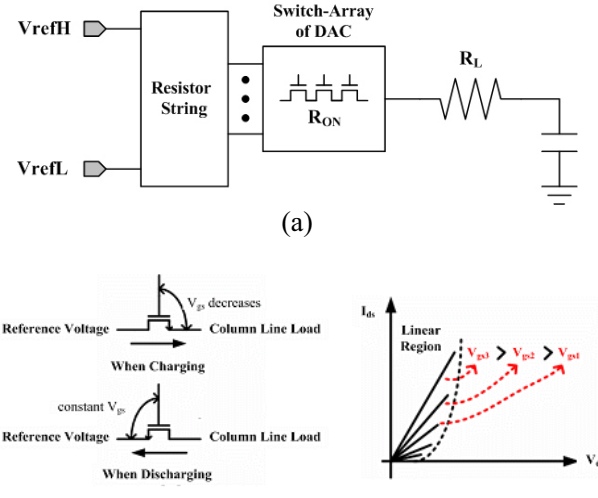

Figure 2. (a) Current path between the reference voltage and the column line and (b) the on-resistance of the TFTs in the DAC when charging and discharging.

of the column line are also represented. The R_{ON} of the TFTs is the factor which there is the difference between charging and discharging time. As shown in Figure 2(b), the source terminal is determined by whether the column line load will be charged or discharged. In case of charging operation, the TFT terminal of the column line side is the source terminal, thus the voltage difference between the gate and the source terminal decreases as the column line load is charged. However, in case of discharging operation, the TFT terminal of the reference voltage side is the source terminal, thus the voltage difference between the gate and the source terminal is constant regardless of the time. Because the on-resistance is the function of the V_{gs}, V_{ds}, W/L, μ, and V_{th}, the average on-resistance with time of the TFTs when charging is larger than that of the TFTs when discharging.

The proposed driving method is to reduce only the charging time only, by boosting the voltage of the column line load to a certain level near the target voltage on the above phenomenon. On the other hand, it discharges a column line load through the DAC which has current path composed with switch-array, thus unnecessary charge waste is reduced and so is the power consumption when discharging operation.

Figure 3 shows the block diagram of the proposed method. The proposed method discharges the previous data voltage to the selected reference voltage of the resistor-string through the DACs. Figure 4 gives a look of the output buffer and the timing diagram.

In the T1 phase, voltage difference between the gate and the source of the TFT 1 is compensated and the column line and the DAC output are connected. Thus, the column line charges or discharges to data voltage using the DAC. However, the voltage of the column line cannot reach the data voltage sufficiently in this phase because of large column line load. In the T2 phase, SW1 switches turn off, and the threshold voltage is stored in the capacitor C1. In the T3 phase, the voltage disorganization of the resistor-string due to the column line charging or discharging is settled down. In the following T4 phase, the buffer charges the column line load around the target voltage because charging the column line load to the target voltage with the resistor-string only is not sufficient due to large amount of the column line load. Finally, in the T5 phase, the column line load gets to the accurate target voltage by connecting the column line with the DAC output. The above operations are summarized in Figure 5.

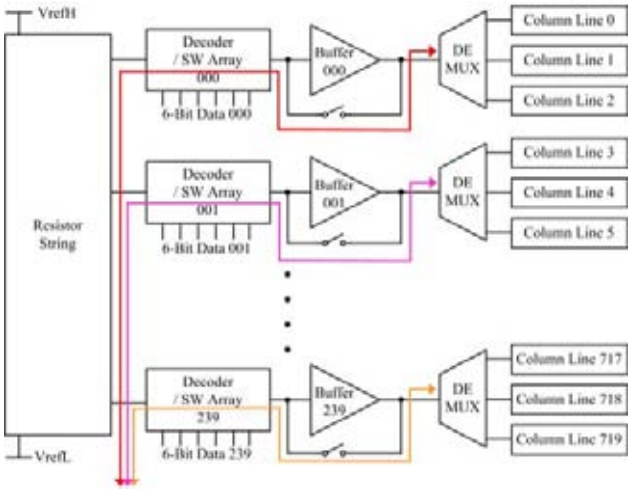

Figure 3. Block diagram of the source driver using the proposed method.

3. Simulation Results

Figure 6(a) shows the output voltages of the DAC and the buffer of the proposed driving method when charging operation under the condition shown in Table 1.

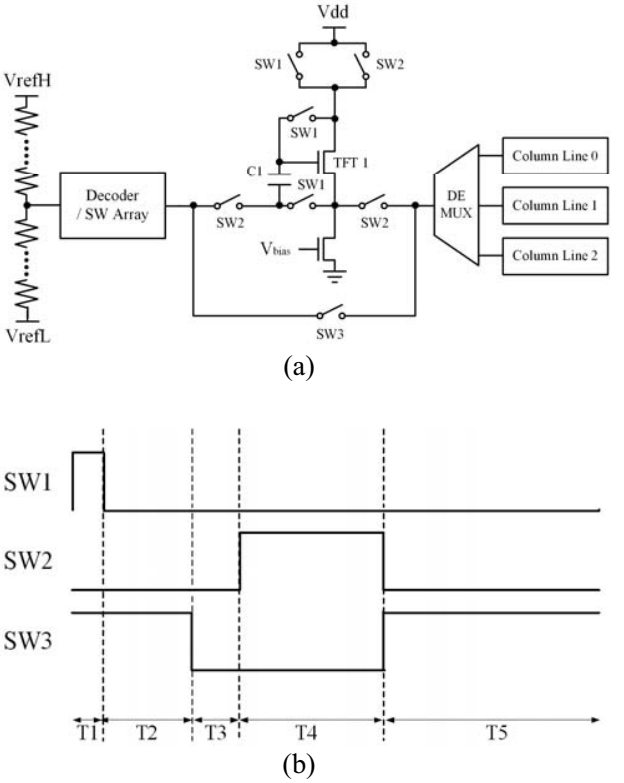

Figure 4. (a) Schematic diagram of the output buffer and (b) its timing diagram for the proposed method.

On the other hand, Figure 6(b) shows the output voltages when discharging operation. In Figure 7, the output error voltages in all gray levels are shown. The outputs of source driver are under 3~5mV error range when the least value of 0.5 least significant bit in the medium grays is 5mV.

Finally, the power consumptions of the conventional method (in Figure 1) and the proposed method are summarized in Table 2. The power consumption of the output buffer is remarkably decreased because the charges of the previous data voltage are reused and pre-charged near the target voltage by connecting the

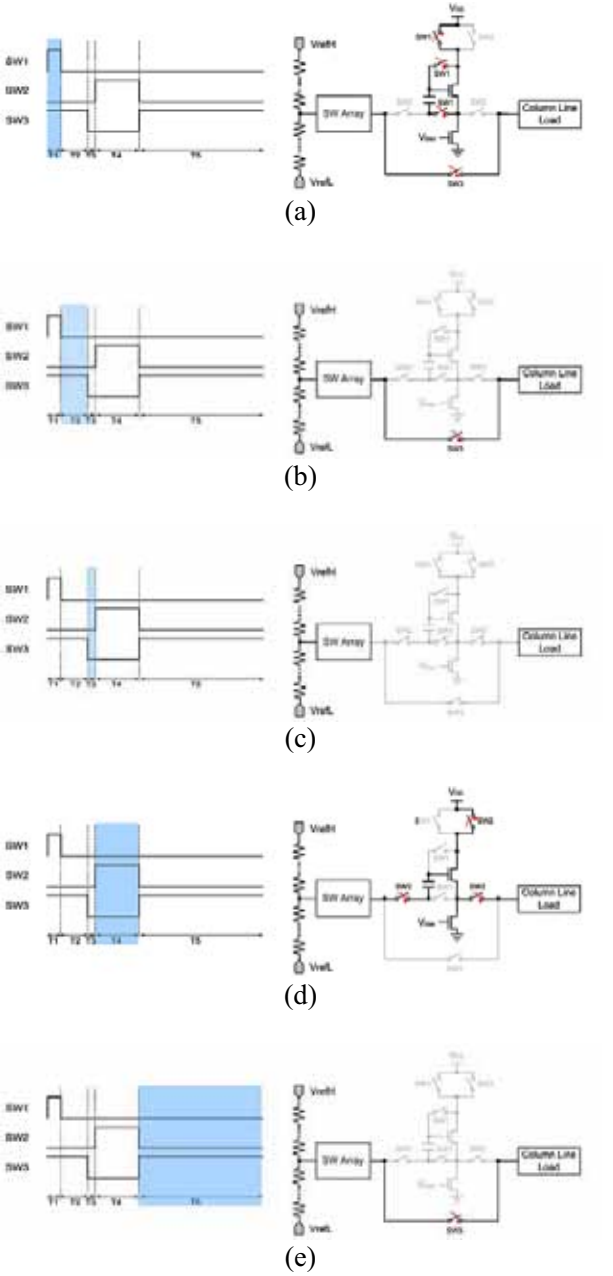

Figure 5. Operation of the proposed driving method: (a) the threshold voltage compensation, (b) charging/discharging the column line load by the DAC, (c) the output settling of the DAC, (d) charging the column load by the output buffer, and (e) the output error compensation.

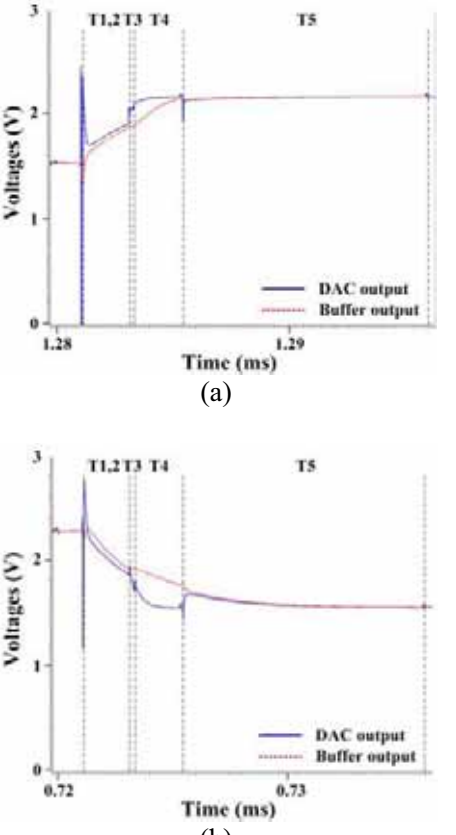

Figure 6. Output voltages of the DAC and the buffer (a) when charging operation, and (b) when discharging operation.

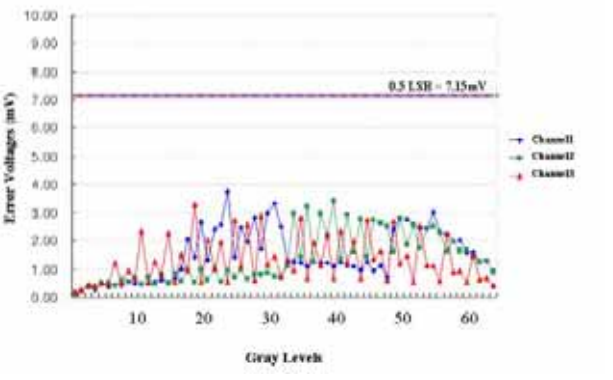

Figure 7. Output error voltages in all gray levels.

Table 1. Simulation condition

Display Resolution		2.2" qVGA (6-bit)
Line Time		15μs (1:3 de-multiplexing)
Range of the Input Voltage		0.7 ~ 3.3V
V_{DD}		-3V, 5V, 7V
V_{TH} Variations	n-channel TFT	1.0 ~ 1.8V
	p-channel TFT	-2.0 ~ -1.1V

Table 2. Power consumption comparison

	Power Consumption (mW)		
	Conventional Method	Proposed Method	
		Maximum	Minimum
Digital Block	3.800	3.800	
DAC	6.760	3.210	0.013
Resistor-String		5.470	2.129
Output Buffer	7.240	1.214	0.261
Total	17.800	13.694	6.193

DAC output to the column line before the operation of the output buffer. The total power consumption of the source driver with the proposed method is 55.9% of that of the conventional driving method source driver.

4. Conclusion

A high-accuracy and low power driving method of the source driver is proposed. The average power consumption of the 240-channel source driver using the proposed method is 9.9mW which is 55.9% of that of the conventional method in 2.2" qVGA LTPS TFT-LCD panel.

5. References

[1] J. Jeon, O. K. Kwon, and I. Lee, “A new digital driving scheme for poly-Si TFT-LCD panels,” in *Proc. 18th Int. Display Research Conf.*, 1998, pp. 425-428.

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