A p-channel LTPS active matrix process for OLED displays using a compensation circuit with three TFTs

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Abstract

We have developed a four mask LTPS TFT p-channel process and fabricated active matrix backplanes based on a pixel circuit with three TFTs and one storage capacitor. Top emitting AMOLED displays have been produced to prove the working principle of the active matrix.

1. Introduction

Low temperature polysilicon (LTPS) thin film transistors (TFTs) are well suited for display applications where inexpensive glass substrates are used. Due to its higher carrier mobility, compared to amorphous Silicon (a-Si), LTPS TFTs are suitable not only to drive OLEDs but also to integrate driver electronics on the panel [1]. As a first step, an active matrix backplane has to be realized to drive the OLEDs. Due to different grain sizes in poly Si layers, the characteristic parameters of LTPS TFTs usually show poor spatial uniformity. The associated variations of carrier mobility and threshold voltage have to be compensated by means of dedicated circuits.

In order to drive a non-inverted OLED with a stable current source, p channel devices are required. In this way, it is possible to connect the OLED's anode to the drain of the driving TFT and its cathode to the ground connection.

A suitable interface between active matrix backplane and OLED stack is essential. Two photolithographic steps are required to create the bottom electrode of the OLED and to separate it from the metallization layers below. In our approach an additional photolithographic step has been employed to overcome limitations related to alignment tolerances, inherent to OLED deposition with shadow masks.

2. Results

2.1. TFT-Fabrication

Our LTPS p-channel TFT process requires four photolithographic steps. First a buffer layer (360 nm SiO_2) and an intrinsic a-Si layer (50 nm) are deposited on a glass substrate by PECVD. After a dehydrogenization step (450 °C), single area excimer laser crystallization (SAELC) [2] is performed at 550 mJ/cm² (wavelength 308 nm, pulse duration 210 ns), at room temperature and in ambient air. Then semiconductor islands are patterned with the first photo mask, followed by PECVD deposition of a SiH_4-N_2O based gateoxide.

MoTa is deposited as gate metallization with DC-sputtering and gates are wet-chemically formed with the second photo mask. The following self aligned creation of drain and source contacts is done by doping of BF_2 ions with an ion beam implantation system at acceleration voltage of 120 kV and implantation dose of 4×10^{15} ions/cm². The gateoxide (100 nm) acts as deceleration layer and the gate (220 nm) as shield for the channel. Integration of the boron into the poly-Si lattice is done with excimer laser activation at 330 mJ/cm². Although this activation energy density is lower than the crystallisation energy density, it is sufficient for activation of the doping agent.

Next step is the deposition of Si_3N_4 as interlayer dielectric, followed by dry etching of vias through both dielectric layers in one photolithographic step, using a third photo mask and two RIE etching steps. The first run (O_2/CF_4 plasma) removes the silicon

nitride with a selectivity of 6:1 to the silicon oxide and gives access to the gate layer. The second run ($Ar/H_2/CF_4$ plasma) removes the rest of the silicon oxide with a selectivity of 3:1 to the semiconductor and gives access to drain and source of the transistor without creating polymers or building an oxide layer on the gate metal.

Before depositing the next metallization layer with DC-sputtering, we perform a sputter etching step with Ar to remove any polymers or native oxide possibly created during or after the dry etching step on top of the doped semiconductor. For the contact metallization we use AlNd. To protect this layer, which would oxidize during the fourth photolithographic step, we additionally cover it with a thin capping layer which does not oxidize during the process and can be etched in the same etchant as aluminum. Finally an annealing step (350 °C) is employed to decrease the sheet resistance of AlNd and to reduce contact resistance between AlNd and doped poly-Si.

2.2. TFT-Performance

We have used two TFT geometries, one for the switching and one for the driving transistors. All switches have a W/L-ratio of 20 µm / 20 µm and are realized in a dual gate structure, i.e. the length of gate is 10 µm + 10 µm. We observed that multiple gate structures have a higher on/off-ratio as reported in literature [3]. The realized transistors reached on/off-ratio of more than 5×10^6 and subthreshold slope of 750 mV/dec. Typical transfer characteristics of the switching transistor are depicted in Figure 1.

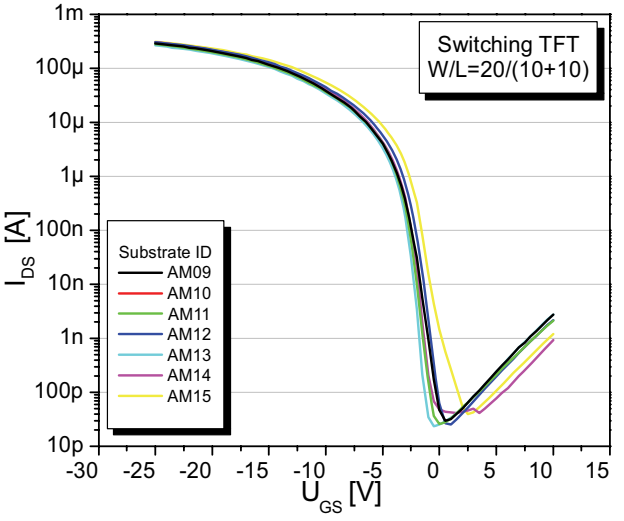

Figure 1: Transfer characteristics of our p-channel switching TFTs

The driving TFTs have a W/L-ratio of 10 µm / 40 µm. This geometry ensures an adequate saturation within the operation region. The devices reach carrier mobility of 40 cm²/Vs and threshold voltage around -4.5 V while the minimum of each transfer characteristic is around 0 V. Typical output characteristics of the driving transistors are plotted in Figure 2.

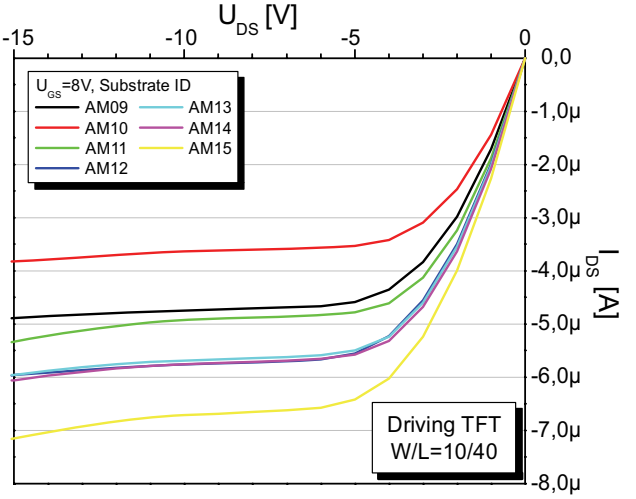

Figure 2: Output characteristics of our p-channel driving TFTs

2.3. Interface AM-OLED

Before depositing the organic layers, three additional photolithographic steps are carried out. First a polyacrylate is spin coated and soft baked. Primarily, this layer is isolating the bottom electrode (anode) from the metallization layers below to avoid unwanted shortcuts. Different from isolating layers already used in the TFT stack, instead of a PECVD layer we use a spin on material here, because in this way we can also level differences in elevation caused by the TFT morphology below and create a smoother surface for the OLED. Then contact holes to the drain of the driving TFTs are exposed and wet chemically developed. To prevent line breaks in this relatively thick planarization layer (≈1,5 µm) the edge of the vias must not be too steep and a melt bake step helps to get the desired flat edges. This step also ensures that any solvent, which may affect the OLED in a negative way, is evaporated.

The next step is the formation of the bottom electrode, where the anode material is deposited with DC-sputtering and structured wet-chemically. Usually to improve the efficiency of the OLED, high

reflective materials are preferred, as in this way light emission to the front side of the display is increased. But for the fabrication of the backplanes other issues were more important, like easy deposition and patterning, good bonding properties and prevention of problems with native oxides built on the electrode before the OLED deposition.

In order to avoid short-cuts between anode and cathode due to the overall in-line process misalignment (mask production, thermal expansion, mask misalignment), finally a step coverage layer of positive non-conductive photoresist is spin coated, soft baked, patterned and hard baked. In this way we also improve the contrast between different pixels, as the step coverage acts like a black matrix in LCD displays.

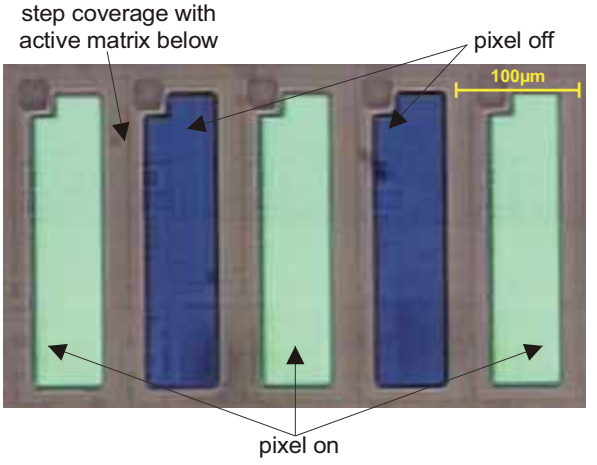

Figure 3: Photo of 5 sub pixels (3 on, 2 off) with step coverage between active matrix and OLED

2.4. OLED Stack

After their fabrication the backplanes were shipped to Novaled to deposit non-inverted top-emitting Novaled PIN-OLEDs™ implementing molecular dopants [4]. The top emission design allows creating a pixel circuit layout without limitations regarding the OLED aperture ratio. The fabrication of the AMOLED display is finished by the deposition of a transparent cathode and the final encapsulation. A cross section view of the presented display is given in Figure 4.

The backplanes support both monochrome and full colour OLED deposition. In order to prove the working principle of the active matrix, three monochrome demonstrators (red, green and blue) have been fabricated. Moreover full colour samples with RGB-pixels structured by shadow mask were prepared. Here, the shadow mask aligning is challenging and needs further improvement.

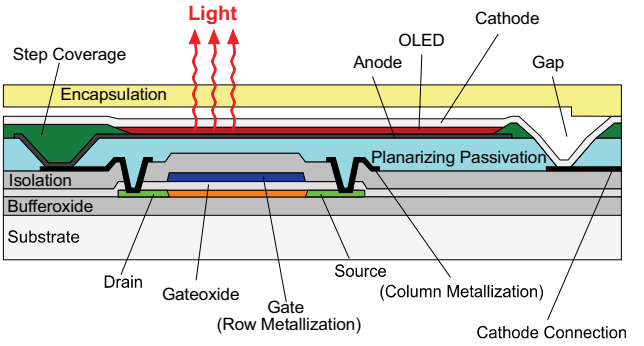

Figure 4: Cross section view of one pixel in the presented active matrix backplane

2.5. Pixel Circuit

In order to drive the OLED a new pixel circuit consisting of three TFTs and one storage capacitor has been developed and patented [5]. The circuit, whose schematic is depicted in Figure 5, has two row control lines (Sel1 and Sel2) and two column lines (Data/I_{FB} and the power supply V_{DD}).

When the second switching TFT Sw2 is off (Sel2 is high), the pixel circuit operates as the standard 2 TFT cell. When the first switching TFT Sw1 is on (Sel1 is low), the data voltage is applied to the gate of the driving TFT Dr1, and the current flowing through the OLED is proportional to the applied data voltage. When Sw1 is off (Sel1 is high), the data voltage is retained in the storage capacitor C_S, which is realized between the row and the column metallization with Si_3N_4 as dielectric.

The second switching TFT Sw2 allows the compensation of threshold voltage and carrier mobility non-uniformities, inherent in the two TFT LTPS pixel circuit. In fact Sw2 enables the measurement of the I-V characteristics of the driving TFT (that is, the current flowing through the OLED) through the Data/I_{FB} column line, allowing the compensation by means of an external dedicated feedback control circuit. The I-V characteristic of the driving TFT can be measured selecting at the same time both switching TFTs and clamping the Data/I_{FB} column line to ground potential (so that there is no current flow through the OLED). An approximated I-V curve can be calculated by means of the measured diode-connected TFT current. This measurement can be performed during the normal operation of the

display using the delay time between two frames. Alternatively the exact I-V curve can be calculated with an iterative measurement method performed as an initial display calibration. During a special test sequence a certain data voltage is applied by selecting Sw1; after deselecting Sw1, the driving current can be measured by selecting Sw2 and clamping the Data/I_{FB} column line to ground potential. The driving current for a stored data voltage can also be checked during the normal operation of the display, selecting for this purpose Sw2 during the delay time between two frames. Because the driving TFT is working in the saturation region, the feedback current I_{FB}, measured clamping the Data/I_{FB} column line to ground potential, is equivalent to the driven OLED current.

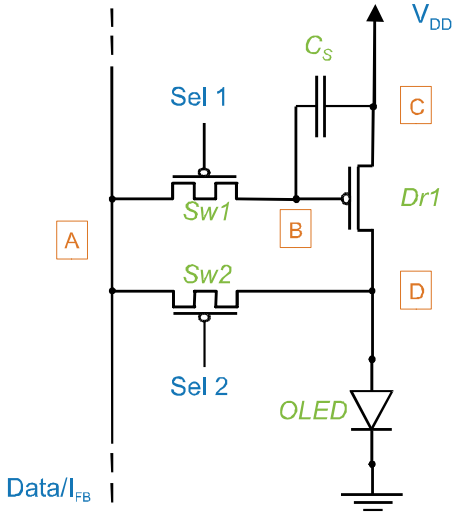

Figure 5: Scheme of the patented 3TFT&1C circuit

The presented 3 TFT pixel circuit allows full access to the pixel driving TFT and even provides the possibility to test the active matrix before the OLED is deposited.

Moreover the additional switching TFT Sw2 gives the possibility to measure directly the OLED forward voltage for a given current. Repeated measurements could keep track of the changes in the OLED characteristic caused by ageing effects.

2.6. Design and Layout

The actual size of the active matrix is 90.2 × 67.7 mm² with a 4:3 aspect ratio. In order to fit 320 × 3 pixels in 240 rows (qVGA) a sub-pixel pitch of 94 × 282 µm² was selected. A photo of the manufactured pixels is shown in Figure 6.

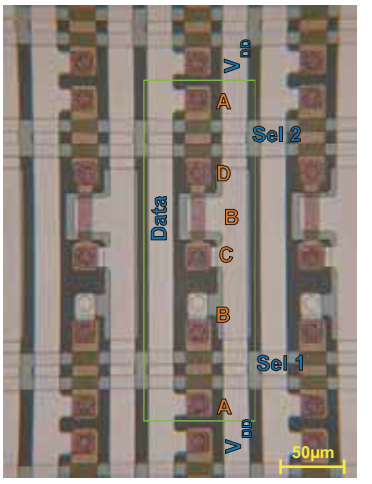

Figure 6: Photo of manufactured 3TFT&1C circuit (without planarizing passivation, anode, step coverage and OLED)

Interconnections for row drivers, source column drivers and compensation column drivers have been implemented. The specifications are summarised in Table 1.

	row	source column	compensation column
driver chip	NEC µPD160702A	Hitachi HD66358	Hitachi HD66358
# of arrays	2 × 240	2 × 480	3 × 160
pad position	lateral sides	top	bottom left
pad length	2.5 mm	2 mm	2 mm
pad pitch	90 µm	52.1 µm	120 µm
pad ratio	45 µm:45 µm	22 µm:30.1 µm	60 µm:60 µm

Table 1: Specifications for drivers and bonding pad arrays

In order to be able to connect the V_{DD} (power supply) and GND (top electrode) wirings by flexible connectors, four couples of 4 × 5mm² patterned (finger like) bonding pads have been placed at the four corners of the demonstrator to ensure uniform power distribution over the entire display.

The drivers were bonded on the active matrix backplane by Thomson and then connected to a versatile, dedicated signal processing setup developed by Deutsche Thomson-Brandt. As the external feedback circuit has not been completely finished yet, the presented displays are operated in the standard two TFT mode.

2.7. Laser Crystallisation Related Defects

As already mentioned we use an area laser, with a mesa shaped laser spot, for the crystallization and get the best device performance with ten shots per area [2]. As the spot size ($68 \times 27\,mm^2$) is smaller than the substrate size ($10 \times 12cm^2$) we cannot process the complete substrate at once. After ten shots at one position, we move the sample to the adjacent position. In this way, we create eight different crystallisation areas. The setup and the spot size of our laser are depicted in Figure 7.

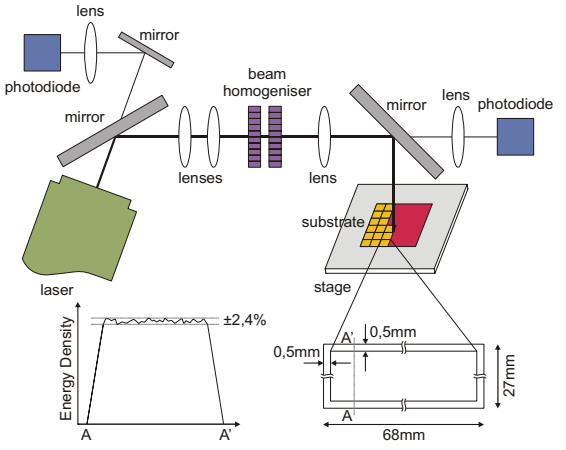

Figure 7: Sopra VEL15 – setup and spot size

Due to the homogeneous energy density within the relatively large laser spot, the diameter of the poly-Si grains is quite uniform and the characteristic stripe patterns, known from line lasers, are not visible, neither in the silicon layer nor in the final display. Nevertheless we need to create an overlap at the border of each laser area which is approximately 500 µm. The eight laser spots can be seen in the silicon layer but also in the final display like shown in Figure 8 (marked with arrows) and Figure 9.

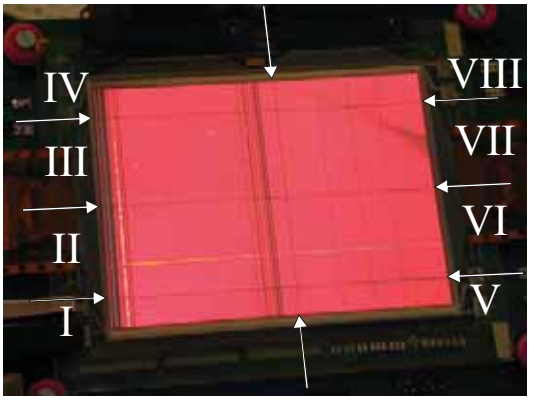

Figure 8: Monochrome red display (fully on)

All TFTs are working properly also those in the overlap area, although they have different threshold voltage and mobility than adjacent TFTs inside one laser spot. But this drawback can be compensated by the feedback circuit while measuring the current through transistor Sw2 and correspondingly adjusting the data voltage.

Another laser related effect, is the difference in luminescence between to adjacent laser spots, visible in Figure 9 (e.g. III and IV). It was already mentioned, that each area is exposed ten times to the laser radiation but not only the average energy density is important but also the energy density of the last shot, which strongly influences the final grain size of the poly-Si. Although the laser energy density is regulated, it is not always possible to ensure equal conditions within all eight laser spots. This also leads to different threshold voltage and mobility of TFTs within adjacent laser spots. Again this drawback can be compensated by sensing the OLED current and adjusting the data voltage within the feedback circuit.

Figure 9: Monochrome green demonstrator with eight laser spots, showing energy density of the last, average and standard deviation of ten shots

2.8. Other Defects

The defect rows and columns, visible in Figure 8 and Figure 9, are caused by difficulties in the bonding process, which is very challenging as the bonding pitch is relatively small. Broken columns are clearly visible in the right half of both displays. Most likely we've corrupted the contact of the first column driver (right half) while bonding the second driver (left half).

Errors like pixels which are always on or always off are also visible, especially in Figure 9, and are caused by restrictions of our photolithography and sometimes by particles. It is not a fundamental problem of the active matrix backplanes.

Within Figure 8 (spot VII) a dark tail is visible on the right side, which was caused by contamination. Most probably the shadow mask has slightly touched the surface of the backplane during its alignment.

3. Conclusion

We have successfully developed a four mask p-channel LTPS TFT process and have fabricated 4.4" full colour qVGA active matrix backplanes with sub pixel pitch of $94 \times 282\ \mu m^2$, implementing a novel pixel circuit with three TFTs and one storage capacitor, allowing compensation of the transistors' spatial non-uniformities. To demonstrate the working principle of the active matrix, we have fabricated monochrome OLED displays with top emitting small molecules. Table 2 shows the properties of our three monochrome displays, at operation voltages of $V_{DATA} = 13\ V - 7\ V$, $V_{DD} = 14\ V$ and $GND = 3\ V$.

	red	green	blue
x coordinate	0.3911	0.6785	0.1554
y coordinate	0.6058	0.3155	0.1291
Luminance [cd/m²]	723.7	67.3	44.79
Contrast	822:1	2243:1	4479:1

Table 2: Display properties (fully on)

4. Acknowledgements

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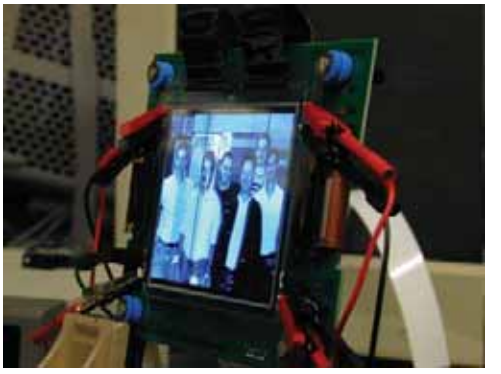

Figure 10: Part of the developer team shown on the monochrome blue AMOLED display

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