New Voltage Programming LTPS-TFT Pixel Scaling Down VTH Variation for AMOLED Display

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Abstract

A new voltage-scaled compensation pixel which employs 3 p-type poly-Si TFTs and 2 capacitors without additional control line has been proposed and verified. The proposed pixel does not employ the V_{TH} *memorizing and cancellation, but scales down the inevitable* V_{TH} *variation of poly-Si TFT. Also the troublesome narrow input range of* V_{DATA} *is increased and the* V_{DD} *supply voltage drop is suppressed. In our experimental results, the OLED current error is successfully compensated by easily controlling the proposed voltage scaling effects.*

1. Introduction

Recently, organic light emitting diodes (OLEDs) displays have advantages such as high brightness and wide viewing angle by self-emissive characteristics [1]. However, the inevitable current non-uniformity of poly-Si TFT arrays due to the threshold voltage (V_{TH}) and the mobility (μ_{eff}) variations, which are caused mainly by crystallization such as excimer laser annealing (ELA), is critical for high-quality images [2-3]. Many pixel circuits have been reported in order to compensate the non-uniform OLED current (I_{OLED}) variation by the voltage or current programming methods [2-6].

In voltage programming method, the pixel panel is easily interfaced with the widely used voltage driver. However, each pixel circuit requires the various considerations for compensating the V_{TH} and mobility non-uniformities of poly-Si TFTs as well as the supply voltage drop in the V_{DD} line [3-5]. The compensation pixel circuits use 4~6 poly-Si TFTs, 1~2 capacitors, 1~3 scan signals, 1~2 supply voltages, typically. Therefore, the large area consumption of the compensation circuit in pixel layout seems inevitable.

Furthermore, although the recent efficiency improvement of the OLED luminance is desirable, it may cause another side-effect reducing the input data range. Since the required current for full-brightness OLED is reduced to 1μA-level, the input voltage range will be determined within 1~2V due to the high-performance of poly-Si TFTs. The small range of the input data would cause the variation error in the OLED current controls. If the input data range is small, the variation effect of V_{TH} is dominant for the OLED current variation. The current variation may be too much severe with regard to the small V_{TH} variation (±15%).

The purpose of our work is to propose a new voltage-programmed pixel design theory employing the voltage-scaled programming. The proposed scheme increases the input data range and compensates the V_{TH} variation. In this paper, the simulation and experimental results successfully verified the proposed compensation theory.

2. Proposed Voltage Scaling Theory

Until now, in the voltage programmed pixel circuits, almost researches have focused on the V_{TH} memorizing and cancellation, which requires rather complicated compensation circuits in each pixel [3-5]. However, based on the improvements of the device process uniformity in the near-future, the V_{TH} variation would be reduced in progress. Therefore, the non-uniformity 'reduction' of poly-Si TFTs rather than the non-uniformity 'cancellation' may be also effective and feasible for compensating the non-uniformity.

In this paper, we propose a new voltage programming method which compensates the current non-uniformity by the voltage scale-down scheme. Fig. 1 shows the proposed voltage-scale driving pixel, which is composed of 3 p-type poly-Si TFTs and 2 capacitors. The transistor T1 is a switch to address the data voltage (*DATA*) to pixel, and T2 is a driving transistor to flow an OLED current by its saturation regime. T3 is a transistor for compensation scheme and gives a capacitive coupling of C1 to the gate node of T2. Each capacitor C1 and C2 is a storage capacitor in parallel pair and the storage capacitance (C_{ST}) is C1+C2. In this circuit operation, the data voltage as well as V_{TH} is modulated and scaled down by the capacitive-coupling through C1 and C2 so that I_{OLED} is scaled down and the I_{OLED} variation is compensated by scaling down the non-uniform current flows.

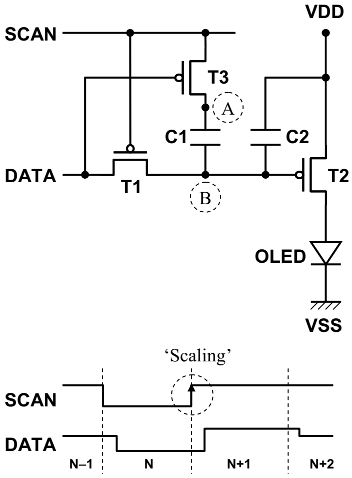


Fig. 1. Proposed AM-OLED pixel circuit (3 p-type poly-Si TFTs and 2 capacitors) employing a voltage-scaled programming

The operation of the proposed circuit is as follows. When the *SCAN* is turned on from V_{DD} to V_{SS} and the *DATA* is still the previous one ($V_{DATA.N-1}$), the voltage (V_A) of node A is set to $V_{DATA.N-1} - V_{TH\_T3}$ by T3 and the voltage (V_B) of node B is set to $V_{DATA.N-1}$ by T1. T3 is turned off because the *SCAN* is V_{SS}. When the present data $V_{DATA.N}$ is addressed now, V_B is changed to $V_{DATA.N}$ and V_A is also changed from $V_{DATA.N-1}-V_{TH\_T3}$ to $V_{DATA.N} - V_{TH\_T3}$ by C1 coupling from the node B. The I_{OLED} flows by T2 without scale-down and is the same with I_{CONV} of the conventional 2-TFT.

$$I_{OLED} = 1/2 \cdot k \cdot (V_{GS\_T2} - V_{TH\_T2})^2$$

$$= 1/2 \cdot k \cdot (V_{DATA.N} - V_{DD} - V_{TH\_T2})^2 = I_{CONV} \quad \cdots\cdot (1)$$

(Here, k is $\mu_{eff} \cdot C_{OX} \cdot W_{T2}/L_{T2}$ and $V_{TH} < 0$)

When the *SCAN* is turned off from V_{SS} to V_{DD}, T1 is turned off. And T3 is turned on at the condition $V_{SCAN} > V_{DATA.N} - V_{TH\_T3}$ during the *SCAN* off-transition. The node A is charged by the SCAN from $V_{DATA.N} - V_{TH\_T3}$ to V_{DD}. It is noted that the node B is capacitively-coupled by the node A fluctuation (V_{fluc}) of $V_{DD} - V_{DATA.N} + V_{TH\_T3}$. Fig. 3-17 illustrates the fluctuation of the node A by capacitive coupling from the SCAN signal. We denote the node B coupling as ΔV_B, then the I_{OLED} is given as follows,

$$I_{OLED} = 1/2 \cdot k \cdot (V_{DATA.N} + \Delta V_B - V_{DD} - V_{TH\_T2})^2$$

$$= 1/2 \cdot k \cdot \{C2/(C1+C2) \cdot (V_{DATA.N} - V_{DD} - V_{TH\_T2})\}^2$$

$$= \{C2/(C1+C2)\}^2 \cdot I_{CONV} \quad \cdots\cdots\cdots\cdots\cdots\cdots (2)$$

Here, the ΔV_B is determined by C1 and C2: $\Delta V_B = \{C1/(C1+C2)\} \cdot V_{fluc}$. And V_{TH} of T2 and T3 is assumed to be same ($V_{TH\_T2} = V_{TH\_T3}$) by the identical line beam irradiation of excimer laser annealing [2,4]. In this equation, the scaling factor (α) is defined as C2/(C1+C2). The I_{OLED} of the proposed pixel is finally scaled-down by a factor of α^2 compared with I_{CONV} of the conventional 2-TFT. If the capacitance C1 and C2 is same, the scaling factor α is 0.5 and the OLED current is scaled down by $0.5^2 = 0.25$ of the conventional one. The current compensation scheme may be analyzed in the equation (2). It is noted that the parameter V_{DATA}, V_{DD}, V_{TH} are scaled down by the scaling factor (α). The fact that the addressed V_{DATA} is scaled down indicates that the V_{DATA} input range is scaled up for the same I_{OLED}. In the viewpoint of V_{TH}, the proposed pixel circuit provides an effective reduction of the V_{TH} variation due to the process variation. If the scaling factor α is 1/3, for example, the inherent V_{TH} variation of ±15% from its average would be reduced to ±5% by a circuit effect.

3. Simulation and Fabrication

In order to verify the proposed pixel circuit, the SPICE simulation and the fabrication were carried out. The SPICE model is RPI poly-Si TFT model (level = 36) and the simulation parameters for TFT and OLED are extracted from the measurements. The low-temperature (450°C) p-type poly-Si TFTs are fabricated by the typical TFT process such as PECVD a-Si film deposition, ELA with line beam laser irradiation, and ion implantation for doping [7]. The size of poly-Si TFT is W/L = 10μm/10μm, and the measured V_{TH} is −2.11V and μ_{eff} is 80 $cm^2/V{\cdot}s$. The OLED is modeled as a diode-connected TFT by fabrication and the threshold voltage of OLED is about 2V.

Fig. 2 shows the I_{OLED} measurement results according to the *DATA* inputs. In the conventional 2-TFT circuit, the *DATA* input required for I_{OLED} = 0~1000*nA* is from 8.6V to 7.4V, thus the data input range is 1.2V. In the proposed circuits, in which the ratio of C1:C2 is 1:1, 2:1, 3:1, it is increased up to 2.0V, 2.7V, 3.3V, respectively. Since I_{OLED} is varied sensitively by ($V_{DATA} - V_{DD} - V_{TH}$), the increased input range of V_{DATA} contributes to suppressing the affect of V_{TH} variations.

Fig. 3 shows the transient curves of voltage node B in the proposed pixel circuit. The node B is changed with respect to 15% V_{TH} variation (± 0.3V), while that of conventional 2-TFT pixel does not change. From the equation of ΔV_B, the change of ΔV_B due to ΔV_{TH} is $\{C1/(C1+C2)\}\cdot\Delta V_{TH}$. If C1:C2 = 5:1 and ΔV_{TH} = ± 0.3V, ΔV_B would be changed by ± 0.25V. It is well consistent that the simulation results of the curve (a) and (c) exhibit ± 0.24V from 7.96V of the curve (b). Therefore, the proposed pixel reduces and compensates the V_{TH} non-uniformity of poly-Si TFTs.

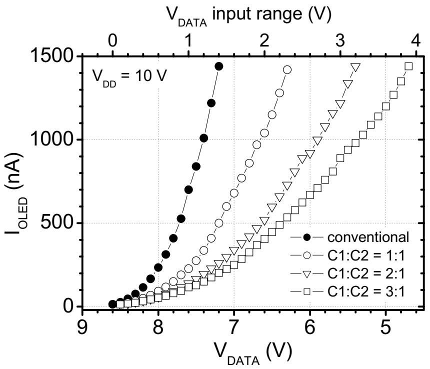


Fig. 2. Measurement results of the pixel current (I_{OLED}) according to the input data voltages in the conventional 2-TFT pixel and the proposed pixel with various scaling conditions (C1:C2 = 1:1, 2:1, 3:1)

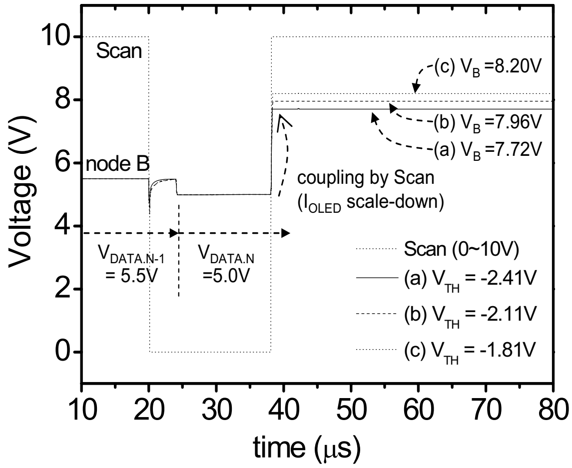
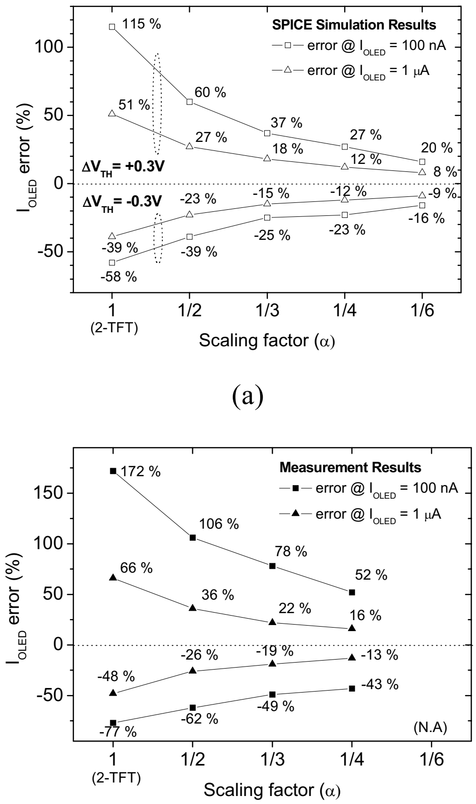


Fig. 3. Simulation results of the voltage node B of the storage capacitor when the same data voltage is addressed to the proposed pixel of C1:C2=5:1 which has a different threshold voltage (a) −2.41V, (b) −2.11V, and (c) −1.81V.

Fig. 4 shows the I_{OLED} error comparison when the V_{TH} of T2 and T3 is varied by ± 0.3V (± 15%) from −2.1V. The I_{OLED} errors were investigated at two reference current levels of I_{OLED} = 100nA and 1μA around. The SPICE simulation results (Fig. 4a) show that, in the conventional pixel of which we can say the scaling factor (α) is 1, the OLED current variation due to +0.3V variation of V_{TH} is 115% at the 100nA level and 51% at the 1μA level, respectively.

In the proposed pixels, the capacitance ratio of C1:C2 is varied from 1:1 to 5:1, thus the scaling factor from 1/2 to 1/6 is determined. The OLED current compensation is improved as the scaling effect is enhanced. When α is 1/6, the non-uniformity of I_{OLED} is considerably reduced to 20% from 115% at the 100nA and no more than 8% from 51% at the 1μA, respectively, compared with the 2-TFT pixel. Because the V_{GS} (= $V_{DATA} - V_{DD}$) for I_{OLED} = 100nA is relatively smaller than that for 1μA, V_{TH} variation portion in ($V_{DATA} - V_{DD} - V_{TH}$) is relatively large and the error would be increased in the small current level.



(a)

(b)

Fig. 4. (a) Simulation and (b) measurement results of the I_{OLED} error comparison in the conventional 2-TFT pixel and the proposed pixel with various scaling factor (α) when the V_{TH} of T2 and T3 is varied by ± 0.3V (± 15%) from −2.1V

The measurement results also present a similar trend with the simulation results as shown in Fig. 4b. To investigate the I_{OLED} error due to ± 0.3V of V_{TH} variation in real device, we use the equivalent measure condition that the V_{DATA} rather than V_{TH} is varied with ± 0.3V in the identical circuit sample, as is reasonable from the equation (2). When α is 1/4, the non-uniformity of I_{OLED} is considerably reduced to 52% from 172% at the 100nA and 16% from 66% at the 1μA, respectively, compared with the 2-TFT pixel. In the expectation from the simulation and the measurement, the error would be reduced below 5% when the scaling factor is optimized.

4. Conclusions

We have proposed a novel compensation scheme employing the voltage-scaled programming pixel which reduces the V_{TH} variation of poly-Si TFT rather than the V_{TH} memorizing and cancellation. By the proposed circuit effect, the V_{TH} is scaled down and the non-uniform OLED current is successfully reduced and compensated. The data input range is also increased by the scaling factor and the current variation sensitivity to V_{TH} variation may be lowered. The scaling factor is easily controlled by the capacitance ratio of C1 to C2. The proposed scheme also contributes to suppressing the V_{DD} drop problem by employing the reported supply line elimination design. The proposed driving theory is promising for achieving uniform image in the voltage programming method.

6. References

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