2.2 inch qqVGA AMOLED drived by ultra low temperature poly silicon (ULTPS) TFT direct fabricated below 200°C

Jang Yeon Kwon, Ji Sim Jung, Kyung Bae Park, Jong Man Kim,
Hyuck Lim, Sang Yoon Lee, Jong Min Kim
Display Device & Material Lab, Samsung Advanced Institute of Technology (SAIT), Yongin, Korea Phone:82-31-280-6934, E-mail: jangyeon.kwon@samsung.com

Takashi Noguchi
Ryukyu University, Okinawa, Japan

Ji Ho Hur, Jin Jang
Dept. of Information Display, Kyung Hee University, Seoul, Korea

Abstract

We demonstrated 2.2inch qqVGA AMOLED display drived by ultra low temperature poly-Si (ULTPS) TFT not transferred but direct fabricated below 200°C. Si channel was crystallized by decreasing impurity concentration even at room temperature. Gate insulator with a breakdown field exceeding 8 MV/cm was realized by Inductively coupled plasma - CVD. In order to reduce stress of plastic, organic film was coated as inter-dielectric and passivation layers. Finally, ULTPS TFT of which mobility is over 20 cm^2/Vsec was fabricated on transparent plastic substrate and drived OLED display successfully.

1. Introduction

Display on plastic substrate is very attractive because it is bendable, rollable and flexible. However, even though it does not flexible, plastic display has a lot of advantage such as thin thickness, light weight and unbreakableness in the view point of mobile use especially [1]. This makes that mobile electronics have compact volume. It is also able to increase using-time of mobile electronics by the increase of battery volume which is reduced by display part, without changing total volume. In order to realize compact volume display, OLED is one of the best approach compared with LCD, because OLED need not backlight unit. Although a-Si TFT can drive OLED, much attention has been focused on poly-Si TFT, because it shows better stability and performance [2].

Poly-Si TFT on plastic has already fabricated by transfer technology [3]. Once poly-Si TFT was fabricated on glass substrate using conventional process, it transfers to plastic substrate. However, it is thought that this technology is not so easy to adapt to large area substrate for reducing cost. In this work, we realized poly-Si TFT array on plastic substrate directly by reducing process temperature to 200°C. In addition, 2.2inch qqVGA AMOLED display was fabricated using 200°C process. In addition, by the reducing process temperature below 200°C, the cost could be reduced by changing substrate from soda-free glass to soda-lime glass or plastic substrate.

2. ULTPS TFT

Figure 1 and figure 2 show schematic cross-sectional view and process flow of AMOLED backplane fabricated below 200°C on plastic substrate respectively. After cleaning plastic substrate, buffer layer was deposited on both side of plastic substrate. The buffer layer between plastic substrate and Si active film was deposited for successful crystallization of a-Si film during excimer laser annealing (ELA) process. On the bottom side, silicon dioxide film was deposited for compensation of stress and silicon nitride film for adhesion between silicon dioxide and plastic substrate. For the active layer, silicon was formed by sputtering process with Xe plasma and crystallized by conventional ELA. After silicon patterning by dry etching process, gate insulator (SiO_2) film was form by inductively coupled plasma chemical vapor deposition (ICP-CVD) at 170°C. Dopant was injected by ion implantation and activated by excimer laser annealing instead of furnace annealing process in order to reduce process temperature. Organic layer which was formed by spin

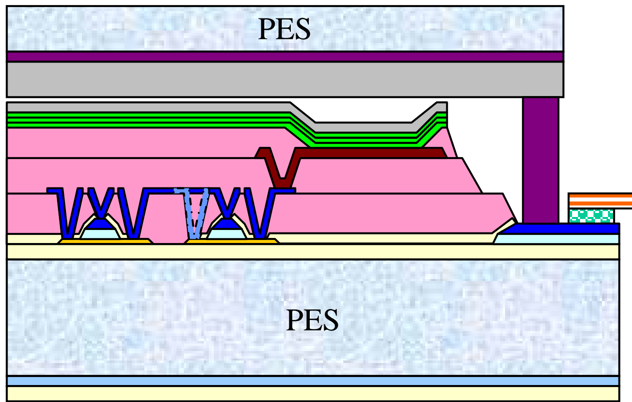


Figure 1 The schematic diagram of AMOLED backplane fabricated below 200°C on plastic substrate

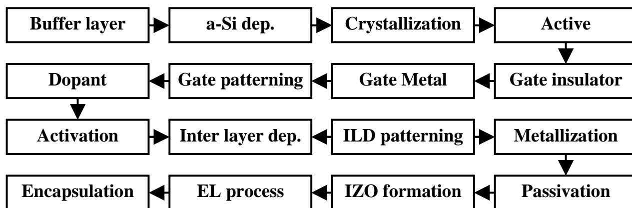
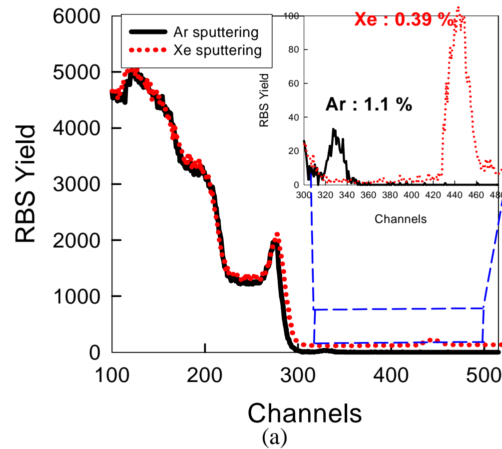


Figure 2 The schematic process flow of AMOLED display fabricated below 200°C

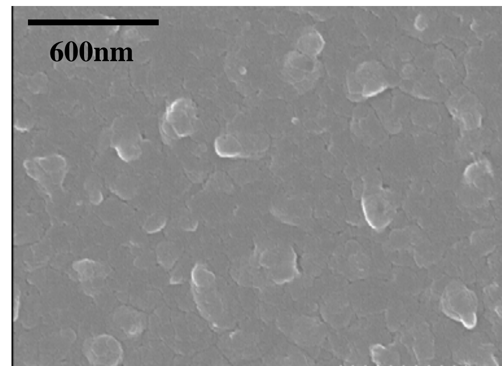
coating process was used for inter-layer-dielectric layer, passivation layer and bank layer in order to prevent plastic substrate bending by the reducing stress. OLED material was thermally evaporated and passivated.

Amorphous Si film as a precursor of active layer was deposited by using sputtering with Xe gas in order to reduce gas concentration in Si film compared with conventional sputtering with Ar gas. As shown in Fig. 3(a), gas concentration in sputtered Si film with Xe gas is lower than that with Ar gas, because it is not so easy for Xe atom to incorporate in film during deposition due to heavier mass compared with Ar gas. This low gas concentration makes it possible to crystallize by excimer laser annealing without Si film delamination from gas evolution. Figure 3(b) shows SEM image of the crystallized Si film.

Even though the delaminating of Si film during laser crystallization was prohibited by reducing gas impurity concentration in Si film, buffer layer properties should be controlled. Figure 4 shows SEM images of crystallized Si film on two kinds of buffer



(a)

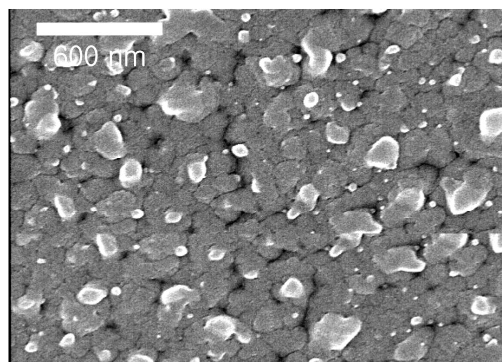


(b)

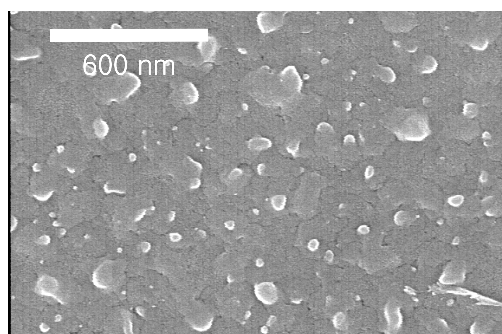
Figure 3 (a) SEM image of Si film crystallized by ELA on plastic substrate. Amorphous Si film was deposited by using sputter with Xe gas. (b) The concentration of gas impurity in Si film was analyzed by RBS. Xe shows lower concentration in Si film than Ar.

layer films. Figure 4(a) shows Si film on relatively rough buffer SiO_2 film and figure 4(b) shows on smooth film. It is thought that the roughness of buffer layer reflect that of Si film directly even though after laser crystallization. In addition, the control of impurity concentration in buffer layer is critical for realizing the active poly Si film for high performance and stable TFT characteristics.

For gate insulator, SiO_2 film was deposited by using ICP-CVD in order to reduce substrate temperature during deposition. Figure 5 shows the variation of current density of SiO_2 film as a function of electric field. Even though SiO_2 film was deposited



(a)

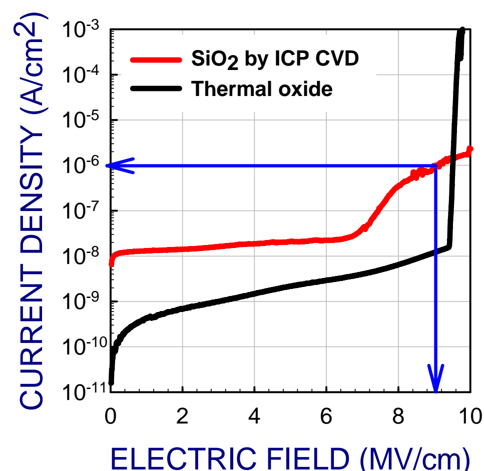


(b)

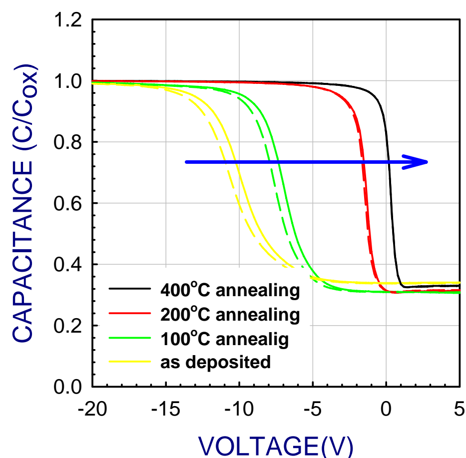
Figure 4 SEM images of poly-Si film by laser crystallization of the sputtered a-Si film (a) with RMS roughness of buffer layer ~ 10nm (b) with RMS roughness of buffer layer ~ 3nm

below 170°C, the breakdown field was measured at 8.6MV/cm which is large enough to realize transistor devices. ICP is one of the high density plasma, so it breaks silane gas effectively even at low temperature

The flat-band voltage of as-deposited SiO_2 film was measured at -11.5V. It is thought that it comes from damage during deposition of metal electrode. This damage can be eliminated by a post annealing of 400°C after metallization, as shown in Fig. 5. 20 minutes is sufficient annealing time for decreasing flat-band voltage. As the annealing temperature increases, the C - V characteristics such as flat-band voltage are improved considerably. The flat-band voltage at annealing temperature 200°C and 400°C were measured by –2V and -0.2V respectively. It is considered that these electrical properties of ICP CVD SiO_2 are sufficiently acceptable for a gate insulator of electronic devices such as TFT.



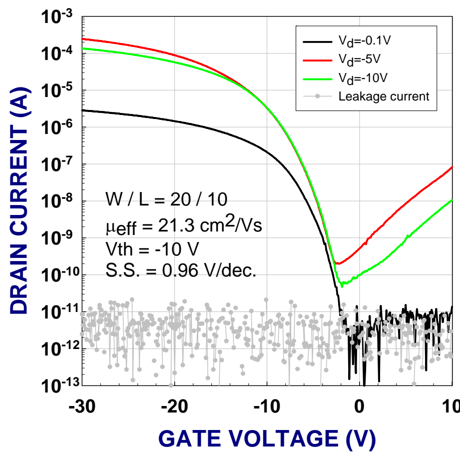
(a)



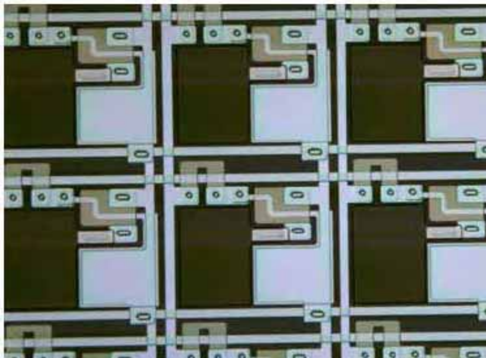
(b)

Figure 5 shows electrical characteristics of gate insulator deposited by ICP-CVD at 170°C (a) current density – electric field curve (b) capacitance – voltage curve

Figure 6(a) indicates typical thin film transistor characteristics fabricated below 200°C. The field effect mobility is over 20 cm^2/Vsec. It is note that the leakage current through gate insulator was measured below 10^{-11} A, even though it formed below 170°C. Figure 7(a) indicates TFT array image fabricated on plastic substrate. 2.2 inch qqVGA (160 x 120) AMOLED display fabricated directly below 200°C shows in Fig. 7(b).



(a)



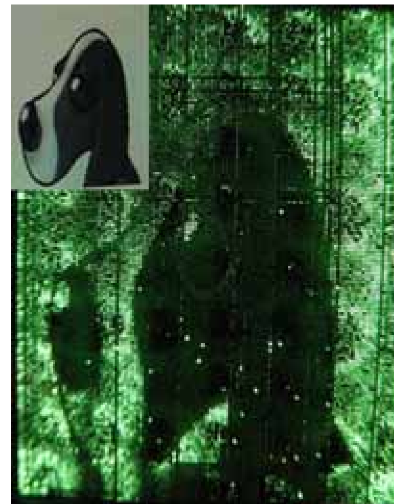
(b)

Figure 6 (a) Typical TFT characteristics fabricated below 200°C (W/L= 20um/10um). (b) Poly-Si TFT image on plastic substrate.

3. Summary

For both high performance and mechanical flexibility, it is essential to realize poly-Si TFT on plastic substrate. Even though the transfer technology could be one of the approaches, it is thought that direct fabrication of poly-Si TFT at ultra low temperature is a more reasonable approach because it is easy to apply large area substrate. We realized AMOLED display using ULTPS TFT array for the first time. This result makes mobile electronics ultra slim, light and unbreakable.

(a)



(b)

Figure 7 (a) Poly-Si TFT array fabricated directly below 200°C on plastic substrate. (b) 2.2inch qqVGA AMOLED display drived by ULTPS TFT array

Table 1. AMOLED Display specification

Item	Specification
Size	2.2 inch (diagonal)
Resolution	120(H) x 160(V)
Pixel Size	273 μm x 273 μm
Color	Mono color
Pixel design	2 Tr & 1C
OLED design	Bottom emission
Aperture ratio	25%
Switching TFT W/L	26/36 (μm/ μm)
Driving TFT W/L	110/10 (μm/ μm)

4. References

[1] N. D. Young, D. J. Mcculoch, R. M. Bunn, “Displays and microelectronics on polymer substrates”, AMLCD Symposium Digest, pp. 47-50, 1997.

[2] M. Stewart, R. S. Howell, L. Pires, M. K. Hatalis, “Poly silicon TFT technology for active matrix OLED displays”, IEEE Trans. on Elec. Dev., Vol. 48, pp. 845-51, 2001.

[3] S. Inoue, S. Utsunomiya, T. Saeki, T.Shimoda, “Surface-free technology by laser annealing (SUFTLA) and its application to poly-Si TFT-LCDs on plastic film with integrated drivers”, IEEE Trans. on Elec. Dev., Vol. 49, pp. 1353-60, 2002.