Low Cost Power System Design for Plasma Display Panel (PDP)

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Abstract

A low cost PDP sustain power supply is proposed based on flyback topology using Boundary Conduction Mode(BCM) to control input current regulation. This method guarantees DCM condition to regulate the input current harmonics under all load conditions. An excessive voltage stress due to the link voltage increase can be suppressed by removing link capacitor and adjusting transformer turns ratios, which makes it possible to be used for universal line applications. The proposed converter is tested with a 400W(200V-2A output) prototype circuit.

1. Introduction

Since AC PDP was invented at the University of Illinois in 1964, the PDP technology has been developed remarkably and it successfully entered Flat Panel Display(FPD) market thanks to its attractive merits such as wide view angle, large screen, high brightness, and thinness. PDP market-share becomes to be widen in large size display market but its cost is still high to compete with other FPDs, which is the most important issue left in PDP to be solved[1]. The operation of PDP is divided into three periods of setup, addressing, and sustaining and its brightness information is defined by sustain pulse number[2]. The sustaining power module takes charge of total power over 80% for sustaining operation.[3] PDP power consumption is controlled by changing the total sustain number according to displayed images due to the low panel efficiency, which causes that the load current drawn by driving circuit is varying according to subfield changes and displayed images. Consequently it is required that PDP sustain power supply should have good voltage regulations under dynamic load changes because the image qualities and discharge margins are seriously affected by the sustain voltage. To meet the requirements, one of the most widely used methods is two-stage method in Fig.1. It has cascade structure comprised of harmonic preregulator to reduce input current harmonics and DC/DC converter to regulate a output voltage. It shows good performances such as high power factor and fast output voltage regulation but increases cost and size due to additional semiconductor switches and control circuitry.

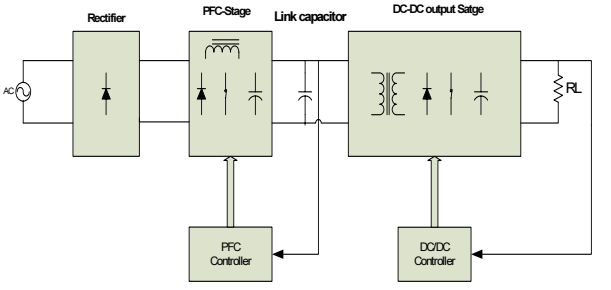


Fig. 1 Two-Stage PFC converter

Another approach is single-stage method, Fig.2, which combines the harmonic regulator with a DC/DC converter into one stage[4]. These converters inherently draw a high quality line current waveform in discontinuous conduction mode(DCM) and have a single control loop to regulate an output voltage. While it has simple structure, this approach has undesirable feature that the link voltage varies according to load conditions because only single control loop exists for the output voltage regulation so that the link voltage is determined by the input-to-output charge-balancing. Most of the single-stage converters that have been studied suffer from this problem, which makes it difficult to use single-stage converters for the applications that require universal input voltage of 90-265V_{rms}. Furthermore, it is difficult to maintain the DCM condition under

dynamic load changes, which increased a heavy current stress.

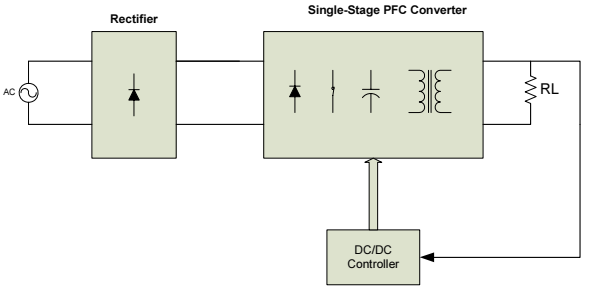


Fig. 2 Single-Stage PFC Converter

In this paper, a low cost PDP sustain power supply is proposed based on flyback topology. By using Boundary Conduction Mode(BCM) to control input current regulation, DCM condition can be met under all load conditions. Another feature of the proposed method is that a excessive voltage stress due to the link voltage increase can be suppressed by removing link capacitor and adjusting transformer turns ratios. Because of increasing switch peak current for BCM operation, switching power loss is increased. To reduce increased switch power loss, a new level-shifting switch driver, which improves the efficiency about 6%, is also proposed. The proposed converter is tested with a 400W(200V-2A output) prototype circuit.

2. Results

2.1 Proposed Converter

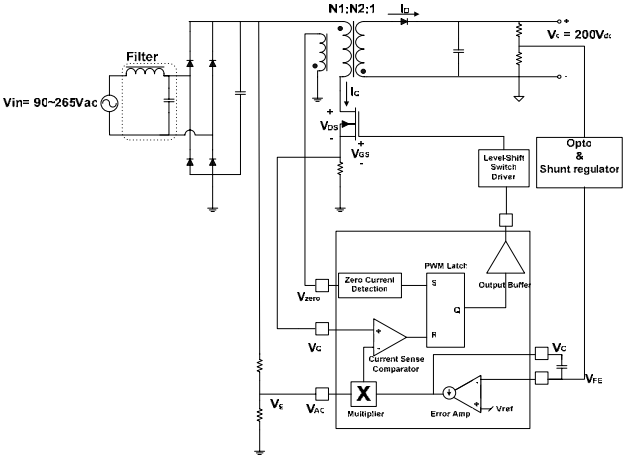
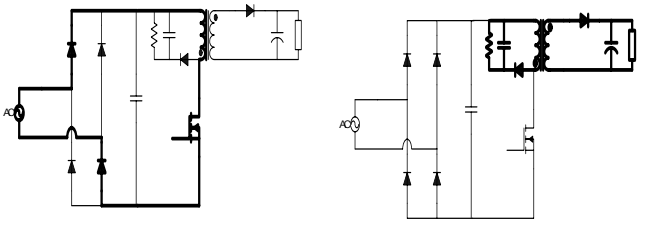


Fig. 3 Circuit diagram of the proposed AC/DC converter

The proposed converter is depicted in Fig. 3. It is derived from basic flyback converter operating in BCM. Four control signals are input to the BCM controller. V_C is the output voltage control signal generated by shunt regulator and V_{AC} is reference signal for regulating input current. Zero detection of the diode current is performed by the voltage of the third winding of main transformer V_{zero} which is used for on-status control of main switch. This signal turns off ZCS operation of output diode current. V_Q is switch current sensing signal. The current command can be made by multiplying V_{AC} and V_C and off status of main switch is controlled by comparing it with V_Q.

2.2 Mode analysis



(a) Mode 1 (b) Mode 2

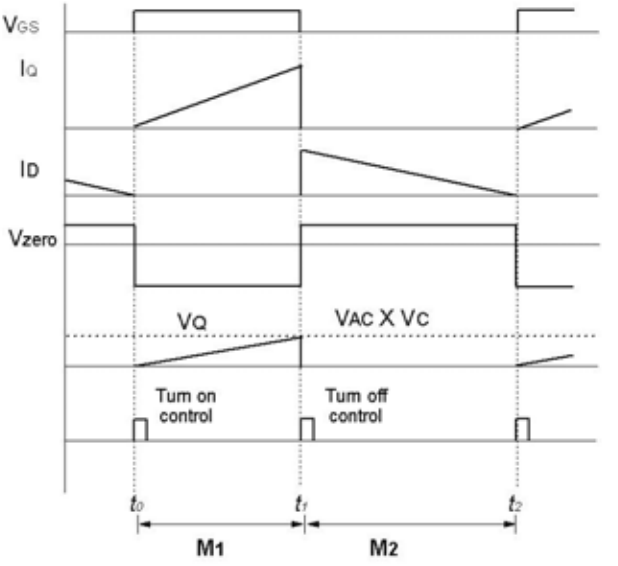


Fig. 4 Key waveforms for mode analysis

Fig. 4 is the operational diagram of the proposed converter.

Mode 1 : $t_0<t\leq t_1$, The main switch is on-state. Then, the main switch current is increased with the slope of V_g / L_1 and the V_Q is also increased. When the V_Q is equal to the current command of $V_{AC} \times V_C$, the main switch is turned off

Mode 2 : $t_1<t\leq t_2$, The charged energy of the main transformer starts to be transferred to the output and the diode current flows with the slope of $-V_o/L_2$ until it becomes zero. If the main transformer is completely reset, the zero detection signal is generated and main switch is turned on again.

Because the current command has the input voltage information, the switch current that is same as input current follows the envelope of the rectified input voltage as shown in Fig. 5. Therefore the filtered input current follows the line voltage without phase shift and shows the similar waveforms.

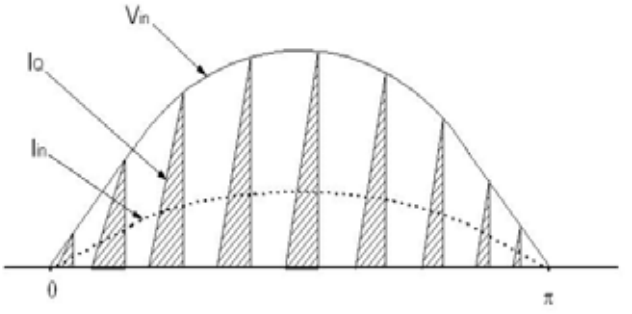


Fig. 5 Line voltage and filtered line current waveforms

In SMPS, MOSFET is generally used as switch, due to its fast switching performance. MOSFET is different from BJT which controls collector current by base current. MOSFET is voltage control source, which controls drain current by voltage between gate and source. MOSFET has parasitic capacitor (C_{gs}) between gate and source. It needs time called turn-on delay time to charge C_{gs}. This is the period of time to charge the gate-source voltage (V_{gs}) to threshold voltage(V_T), and the turn-on delay time can be written as :

$$\tau_{d(on)} = R_G \times C_{gs} \qquad (1)$$

After V_{gs} is equal to V_T, MOSFET changes its operation from active region to saturation region. It takes time for V_{gs} to be V_p (pinch-off voltage) and that is defined rising time t_r. MOSFET in saturation region continues to saturate and it starts to cut off if input voltage(V_{gs}) falls to zero. It is turn-off delay time to discharge V_{gs} to V_p, which is defined by :

$$\tau_{d(off)} = R_G(C_{gs} + C_{gd}) \qquad (2)$$

It is falling-time(t_f) that V_{gs} charged in input capacity takes the time to discharges from V_p to V_T.[5] These switching time constants determine the MOSFET switching speed and switching loss. The prior way to drive MOSFETs was to use Push-Pull Class B Amplifier that can draw peak currents by keeping low output resistance. However, switching turn-off delay time is still hundreds nanosecond because turn-off voltage level of Push-Pull Class B Amplifier does not fall down under zero. To reduce this switching loss, charging and discharging time of C_{gs} should be short. The longer charging and discharging time means extension of coexisting time of current and voltage. It directly causes switching loss that can be a cause of emitting heat and destroying MOSFET. It also affects to the whole system efficiency. Proposed converter can increase switching current by operating BCM. This is a cause of increasing switching loss according to the extension of turn-off switching loss area. To reduce switching-off time can be made by giving negative driving voltage.

2.3 Proposed Level-shifting switch driver

Fig. 6 is a diagram of level-shifting driver, where V_Z means the shifted voltage to increase the turn-off speed. Despite that the turn-on driving voltage is lowed due to the voltage-level shifting, the turn-on loss is not increased because the converter operates in BCM. This operation can be accomplished by the circuit in Fig. 7. S_1 and S_3 are charge-pumping transistors to make positive and negative driving voltage source with storage capacitor C and S_2 and S_4 are gate-driving transistors to apply gate pulses. Capacitor C_{LS} and zener diode D_Z determines the negative shift voltage of base driving pulse of transistor S_2 and S_4. Also additional resistors are current limiting resistors to protect devices

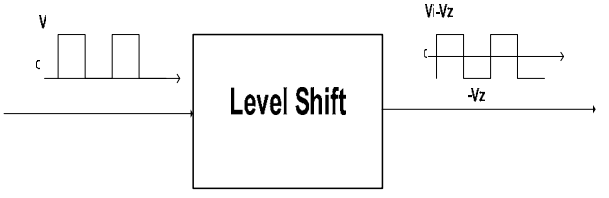


Fig. 6 Block diagram of Level-Shift

Fig. 8 is the key waveforms for mode analysis of level-shifting switch driver. If S_1 and S_2 turn on, the capacitor C is charged to V_S through D and V_S-V_Z is applied to the bases of S_2 and S_4. Then S_2 is turned on and the C_{gs} of MOSFET begins to charge from $-V_Z$ to V_S-V_Z. Next if S_1 and S_2 turn off and S_3 and S_4 turn on at the same time, the voltage level of S_4 collector is $-V_S$ and $-V_Z$ is applied to the bases of S_2 and S_4. S_4 becomes to be turned on and the negative voltage is applied to MOSFET Gate. Because this negative driving pulse discharge the MOSFET capacitance quickly, the turn-off switching speed can be increased.

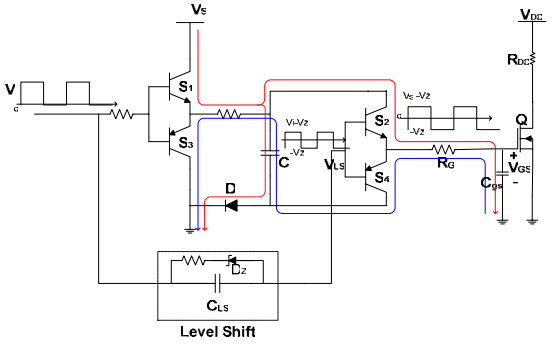


Fig. 7 Circuit diagram of the proposed Level-shift switch driver

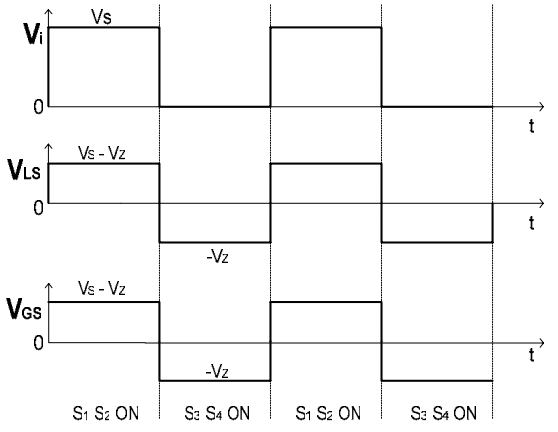


Fig. 8 Key waveforms for mode analysis of level-shifting switch driver

2. Experiment

Table 1 shows the conditions to experiment. The main switch is FQA24N60(600V,24A $R_{ds,on}$ =0.24Ω), the output diode is FES16JT, the core of transformer is EER4950. To reduce the switching loss, we used the level-shifting switch driver. The proposed converter is tested with a 400W(200V-2A output) prototype circuit

Table 1. The specifications for single-stage power module

Input Voltage	AC 90 ~ 265 [Vrms]
Output Voltage	**200 [Vdc]**
Output Power	**400 [W]**

Fig. 9 is the result of the power factor according to line voltage and the load change. If load is over 30%, the power factor can be high as over 0.96 at the universal line voltage. Fig. 10 is the result of the efficiency according to line voltage and the load change. If it is full load, the efficiency is about 87%. Fig. 11 is the waveform of each part of the proposed circuit. The output diode shows the operation of ZCS. The switch current operates as BCM and follows the rectified input current shape. This means good power factor can be obtained. Fig. 11(i) is the stable output voltage waveform at the time of the dynamic load change. This stable voltage can be applied PDP sustaining power module. Fig. 12 is the waveform of switch current and switch voltage when using the prior push-pull switch driver. Fig. 13 is the waveform of switch current and switch voltage when using the new level-shifting switch driver. We reduced switching speed to 200nsec and it is about one third of 720nsec when using the push-pull switch driver, by using the level-shifting switch driver.

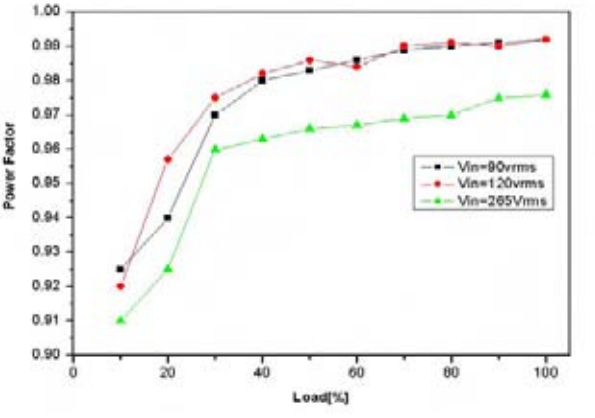


Fig. 9 The measured power factor under line and load variation

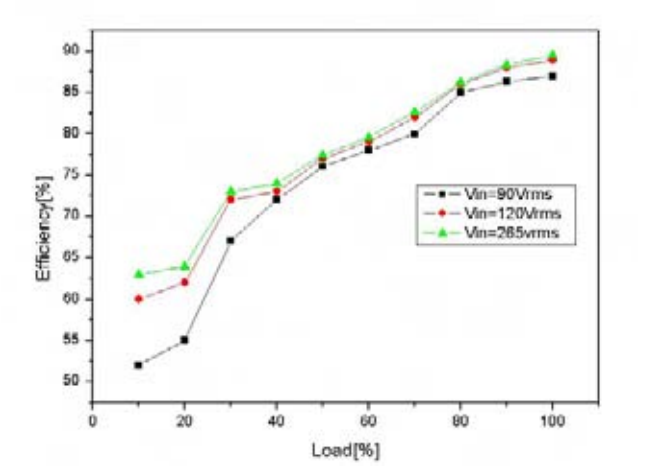
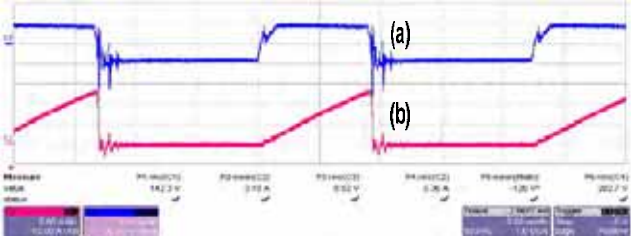
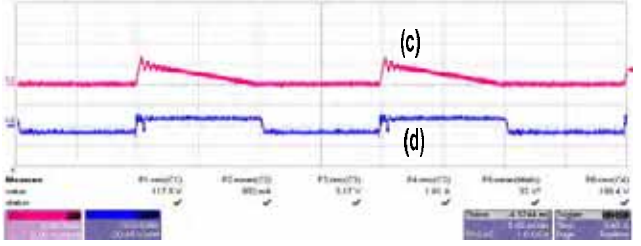


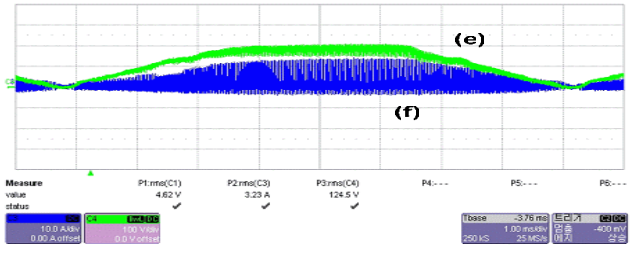
Fig. 10 The measured efficiency under line and load variation



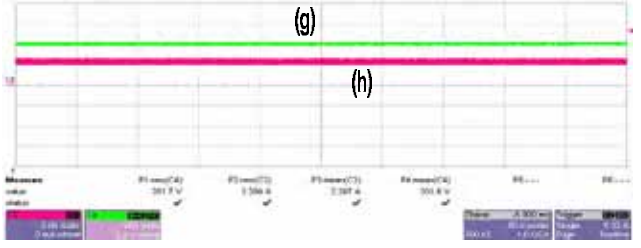
(a) V_{GS} (10V/div) (b) I_Q (5A/div)



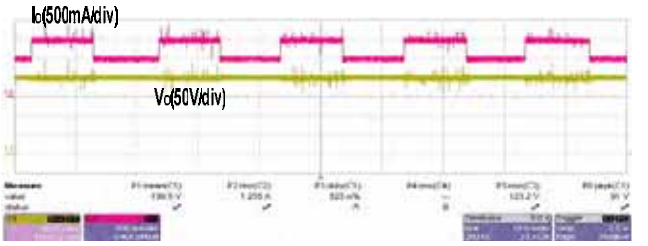
(c) I_D (5A/div) (d) V_{zero} (10V/div)



(e) Line voltage(100V/div) (f) I_Q current (10A/div)



(g) V_O(100V/div) (h)I_O(2A/div)



(i) Dynamic load changes

Fig. 11 Experimental waveforms

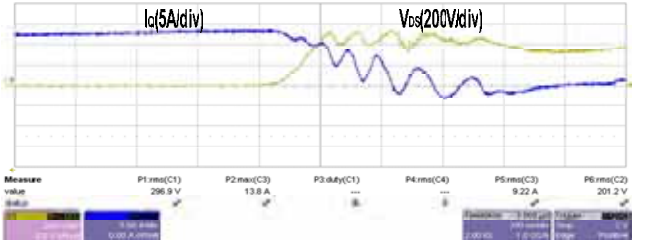


Fig. 12 Waveforms of switching loss of conventional push-pull switch driver

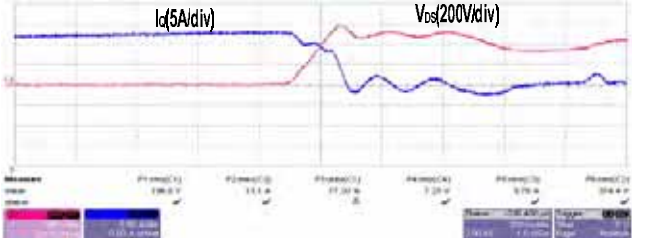


Fig. 13 switching loss waveform when using new level-shifting switch driver

4. Conclusion

In this paper, we propose single-stage PFC flyback converter using for low price PDP power module by BCM control. This method reduces line input harmonic distortion, and it can be satisfied with all load conditions by stabilization of output voltage. In addition, it is satisfied with the condition that output voltage of PDP sustaining power module should keep stable voltage at the time of dynamic load change. It improves the efficiency characteristic about universal input voltage(90~265V_{ac}). We developed the new level-shifting switch driver, so that reduced switching loss. The proposed circuit can reduce the number of device of the complicated circuit which two-stage PDP power supply has at the FPD market. So that, the volume of a board can be reduced and it can reduce

the production cost. Therefore, the proposed converter reduces line input harmonic distortion and works as good output voltage regulation, can also be suitable for low price PDP power module because it reduce the volume of the prior circuit.

5. References

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