High-voltage and low power consumption driver for an electronic paper

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Abstract

A custom-made display driver for an electronic paper is presented, which has high-voltage multilevel output capability and extremely low power consumption. An original level-shifter circuit can effectively reduce the power consumption and the chip area. This driver was implemented to a Quick-Response Liquid Powder Display (QR-LPD) and the image quality and power consumption was estimated.

1. Introduction

Recently, many kinds of technologies for achieving an electronic paper were investigated and the markets using these technologies are about to take off. Within this year, some products will be shipped to the marketplace which is the special one and different from an ordinary marketplace that the LCD has.

That is thought to be the marketplace where the paper media is digitalized, for example, digitalized price tag, signboard or poster with a paper media. In these applications, low power consumption is strongly requested rather than a moving image feature. All the candidate technologies for an electric paper have a bistability or no power consumption after updating the contents in principal, but they are still requested to be extremely low power consumption even in updating in order to reduce the install cost of the power system. In this point, the reduction of power consumption in the driving circuitry of electronic paper is very critical.

Usually a high voltage is needed for driving the bistable displays, for example, Quick-Response Liquid Powder Display (QR-LPD) [1,2], electrophoretic display (EPD) and Cholesteric LCD (Ch-LCD) even though the driving voltages are getting lower as the developments are progressed. Unfortunately, to handle the high voltage needs relatively high power consumption in comparison with the drivers that handle low voltage for logic signals because the high voltage makes the power consumption higher although the transistors have the same leakage current or the gate capacitance as those of low voltage transistors. In addition, the high voltage MOS transistor (HV-MOS) like LDMOS generally needs a large chip area, which leads a higher chip cost. Therefore, the design with fewer HV-MOS as well as low power consumption is expected.

In this paper, we focused on the QR-LPD as an example of bistable displays. Almost all the bistable displays are driven by a passive-matrix addressing except EPD that needs an active-matrix addressing, and need a high driving voltage, so that the following discussions can be applied to other bistable displays. We firstly discussed how much energy is consumed to drive QR-LPD in the system including the driving circuit. None of the bistable displays needs a power except the updating and the updating time does not have to be so short because of a static image. Therefore, the energy per an updating (J) should be employed rather than the power (W). Secondly, we introduce the circuit technology employed in our custom-made driver LSI, which has 160 outputs, the output voltage as high as 110V and the three output levels. The middle output level can sink and source the current to achieve high speed switching. The special level shifter circuit is used to reduce power consumption. Finally, the consumed energy to update the one image was argued by measuring and simulating the circuit.

2. Energy consumption

Figure 1 shows the simplified schematics of the driver circuit and the load capacitance as an equivalent circuit of the panel. The driving circuit for QR-LPD basically needs the three-voltage-levels for both column and row drivers and the middle voltage outputs must have current source and sink functions depending on the voltage of the load capacitance in order to obtain the fast transient of the panel voltages.

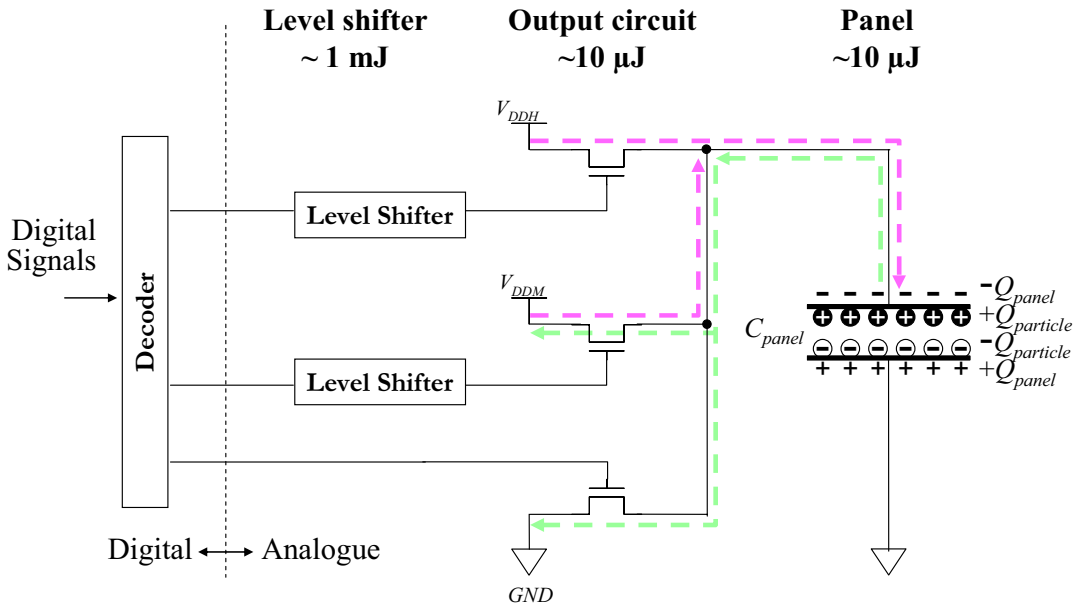

Figure 1. Energy consumption in QR-LPD system.

The panel can be regarded as a simple capacitance if there is no movement of the particles.

When the panel capacitance, C_{panel}, is charged by the high voltage, V_{DDH}, the charge, $Q_{panel}=C_{panel}\cdot V_{DDH}$, is accumulated at the electrodes of the panel. The energy saved in the capacitance is corresponding to $Q_{panel}\cdot V_{DDH}$ / 2, and the same amount of energy is dissipated at the resistance on the transistors or electrodes when the current to charge up the capacitance flows. The saved energy in the capacitance is dissipated when the capacitance is discharged on the resistance on the transistors or electrodes. As a result, the energy, $Q_{panel}\cdot V_{DDH}$, is dissipated in the output circuits for each charging and discharging cycle, and it cannot be avoided irrespective of the output resistances. Some of the energy, however, can be recovered to the middle voltage source. The energy is roughly calculated to be 10 µJ assuming the 10 cm×10 cm panel size, 50 µm gap distance, 70 V applied voltage and 8.85×10^{-14} F/cm vacuum permittivity.

When the particles move in the gap, some energy is consumed. The amount of particle charge is experimentally evaluated to be in almost the same level as that of capacitance charge in QR-LPD. Assuming that $Q_{panel}=Q_{particle}$, the energy dissipated by the moving particles is also calculated to be 10 µJ. However, these energies are negligibly small comparing with that consumed in the level shifter circuit. In our custom driver, we obtained the energy value of about 1 mJ which is consumed in the level shifter circuit for one updating of the same sized panel as discussed before. The level shifter circuit was specially designed to reduce the power consumption as mentioned later. However, it still occupies a large part of whole energy consumed in the system. This fact shows that the design of level shifter is one of the most important parts in achieving the electronic paper with a low-power- consumption. The other part that loses a large energy is the high voltage generation circuit, but it will be discussed in the other future paper.

3. Level shifter circuit

Figure 2(a) is the simplest level shifter circuit. This circuit is composed of four HV LDMOS (lateral double diffused MOS) transistors. Usually LDMOS needs a very large area to hold a high voltage between source and drain because of a large drift region around the drain. In addition, the gate-voltage of HV pLDMOS transistors change between 0 and V_{DDH}. Therefore, the gate and output voltages swing fully, and the insulator must endure a high voltage of V_{DDH}, which requests a thicker gate insulator and additional process leading to cost-up. Moreover, such large voltage swing gives damage to the insulator. To solve these problems, the level shifter circuit in Figure 2(b) is commonly used, where the cross-coupled LV pMOS transistors in a HV nWELL are added and some bias voltage to the gate of HV pMOS. The

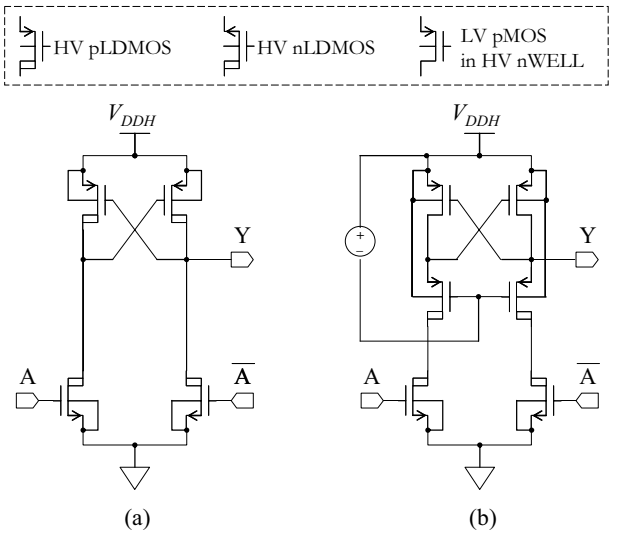

Figure 2. Conventional level shifter circuits. (a)Full swing, (b)Reduced swing modes.

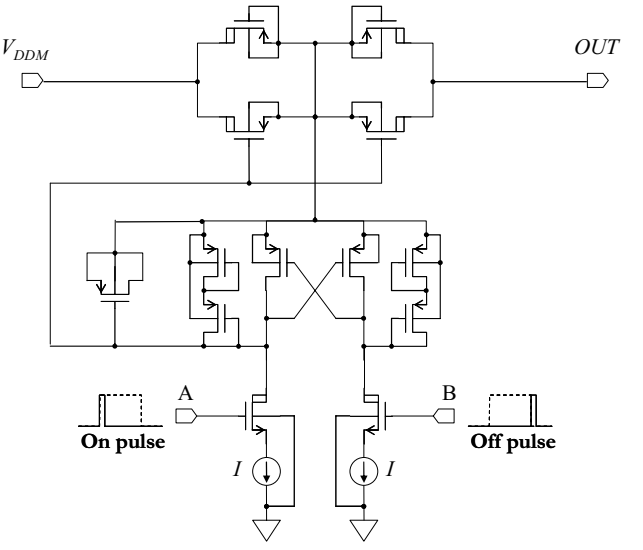

Figure 3. New level shifter circuit with small number of HV-MOS.

voltage applied to the pMOS transistors are reduced to the level of bias voltage. As a result, the same thickness insulator as that of the logic transistors can be used, and the process is simplified resulting in a cost-down. The increase of transistor number does not affect so much the chip area because the LV pMOS in HV nWELL is much smaller than LDMOS. This level shifter needs a bias circuit, which requires some area on a chip and consumes a power. These problems, however, are not so critical since the bias circuit can be shared among some level shifter circuits.

Since the floating pWELL structure gets difficult in such a high voltage process, we cannot use the HV nLDMOS for the output transistor at middle voltage level. Therefore, the output circuit at the middle voltage level gets very complicated as shown in Fig. 2. In addition, the level shifter connected to the output circuit must generate the voltage just several volts below the load voltage that changes with fast transient by sinking the current. Therefore, this commonly used level shifter circuit in Fig.2 (b) cannot be employed because the bias circuit must be shared by each output circuit.

To solve this problem, we investigated a new level shifter circuit as shown in Fig.3. This level shift circuit does not have a bias circuit but the voltage swing is restricted within the breakdown voltage of the thin insulator by putting two diode-connected transistors. When this output transistor turns on, HV nLDMOS of the left side is on, and some current flows through these transistors. These transistors give some voltage according to the flowing current. We designed the transistor dimension and current level not to over the breakdown voltage of the gate insulator. When the output transistor turns off, we make the n-channel LDMOS of the right side on. Then the cross-coupled transistor of left side is on and the output transistor gets off. Since the HV pLDMOS in this level shifter circuit is not needed in this level shifter, we can save the chip area a lot.

However, in this circuit there remains the serious problem that DC current dissipates a lot of power. To save the DC current power dissipation, we cut the DC current by turning off the nLDMOS transistors immediately after adequate short on time. After cutting the DC current, the gate voltage of output transistors is discharged though the diode connected transistors until twice of threshold voltage. Therefore, the output transistor keeps on by this voltage. The capacitance with an adequate value is also added in order to lengthen the discharge time by sub-threshold leak current. The on and off pulses are input to terminals A and B, respectively. Adjusting both of the pulse width and the constant current level can reduce the power consumption at minimum.

The LV pMOS transistors in HV nWELL can exist in the same well of output HV pLDMOS transistors and the size is as small as a low voltage transistor. Therefore, the circuit area is mainly determined by the number of LDMOS transistors.

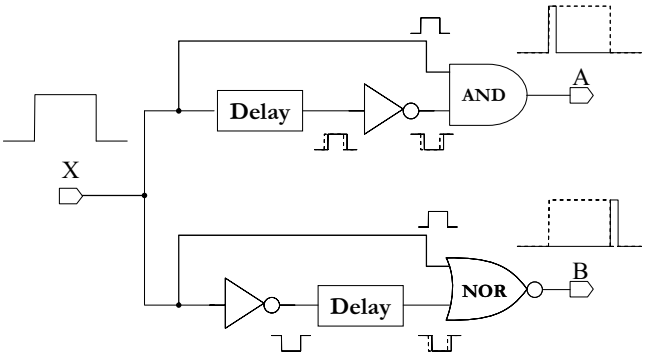

Figure 4 Analogue pulse generation circuit.

This new level shifter circuit is simpler, and needed fewer HV transistors than that used before [1], which helps the smaller circuit area and lower chip cost.

4. Pulse generator circuit

Figure 4 shows the analogue-pulse-generator circuit to input the pulse signals to the level shifter. To change the pulse width, the delay time is modulated by changing CR time in delay circuit block. Another method using the counter circuit can be considered, but digital pulse generation circuit needs higher clock frequency, which causes more power dissipation and needs expensive process with a finer design rule. This simple pulse generator circuit works well and save the cost.

5. Custom driver LSI

According to the above-mentioned circuit technology, we have designed and fabricated the driver LSI using the 0.64μm CMOS/LDMOS High-Voltage (110V) process. The driver LSI has 160 outputs and three voltage levels, that is, high voltage, the middle voltage and the ground voltage in addition to the Hi-Z state. The current sink & source functions were implemented in middle voltage-level outputs. The chip picture that has a long shape with 2.3mm × 21.4mm is shown in Fig.5 (a). Figure 5 (b) is a close-up picture, which shows that more than half area of the chip is taken by high voltage transistors. This driver was implemented to QR-LPD [4].

6. Conclusion

We have developed the custom LSI driver that can be applied to electronic paper that needs high voltage to drive. Using this driver, we could obtain higher quality image and lower power consumption that have never been obtained using the two voltage level driver on QR-LPD. This work extends the electronic paper application area in price tag, electronic signboard or poster because of a long lifetime with battery power supply or solar cell battery.

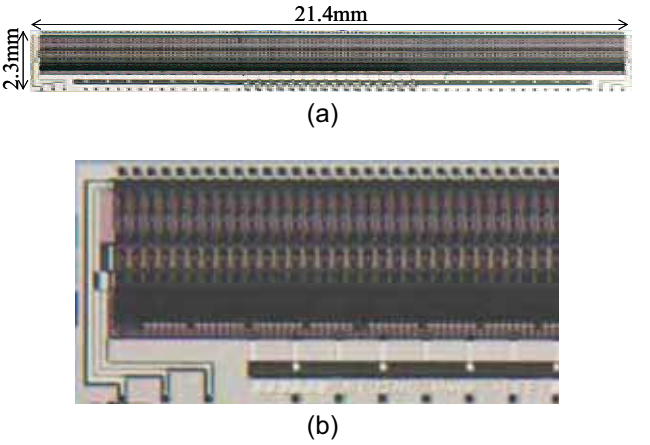

Figure 5 New level shifter circuit with small number of HV-MOS.

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