An Area Efficient 8-bit Current DAC for Current Programming AMOLEDs

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Abstract

This paper presents an area efficient 8-bit current digital to analog convector (DAC) which is applied to 240 channels Active Matrix - Organic Light Emitting Diode (AMOLED) data driver. The proposed circuit constitutes 4-bit binary weighted current DAC and 4-bit switched capacitor cyclic DAC. The proposed DAC has about 70% smaller area than that of the typical binary weighted current DAC. We overcome sampling time by reducing the number of repetition phases so that it can display 8-bit gray scale image.

1. Introduction

The structure of current programming AMOLED data driver IC can be divided into two types according to DAC structures. One is the current sample and holding method with just one DAC, and the other is the typical well known type that each channel has its own DAC.

Figure 1 shows a block diagram of the AMOLED data driver circuit using sample and hold circuit. Each channel of the S/H circuit stores output current data of DAC (Digital-to-Analog Converter) and outputs the stored current. This structure needs high-speed DAC and high-speed S/H circuit to store analog current signal in each channel, because the structure has to operate the data to all channels during line time by one or several number of DAC. However this structure has a problem which shortens S/H (sample and hold) time when the resolution format increases. Moreover it has a problem which is hard to S/H several hundreds nano-amperes level of analog current in high-speed.

Figure 2 shows a block diagram of the AMOLED data driver circuit using DACs built-in in each channel. This can solve the problem of lack of S/H time when using one DAC as Figure 1. Also, it doesn't need output stage for S/H because channel current source supplies continuous current to channel, and it has a merit that it doesn't have to suffer from switching

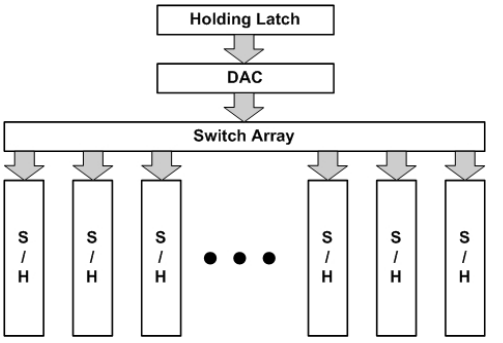


Figure 1. The block diagram of AMOLED data driver circuit using S/H circuit

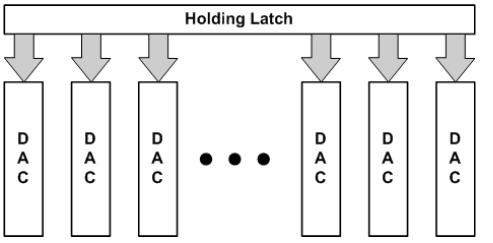


Figure 2. The block diagram of AMOLED data driver circuit using DAC built-in in each channel

error due to the current switching by S/H operation.

In this kind of DAC structure, binary weighted current DAC is generally used for current programming AMOLEDs by using DACs built-in in each channel [2]. Though binary weighted DAC has advantages that it can generate output current and has simple structure, it has a disadvantage of area efficiency. The area of binary weighted DAC circuit doubles when one bit of gray scale increases.

Current cyclic DAC can be used to improve area efficiency instead of binary weighted DAC [1, 3]. The current cyclic DAC needs 3-phase operation to perform one cycle operation to

generate data of 1-bit gray. To display 8-bit gray scale image, however, it sometimes has to sample a small amount of current about a few nano-amperes. In that case, there is no enough time to charge the low current in a capacitor.

To overcome disadvantages of the previous current cyclic DAC, we propose a new area efficient current DAC circuits.

2. Proposed circuit

The schematic diagram of the proposed DAC is shown in Figure 3(a). The circuit constitutes a 4-bit binary weighted current DAC with current source and a cyclic DAC which consists of switched capacitor transistors and diode connected transistors.

In current cyclic DAC, operation is divided into 3 phases as shown in Figure 3(b). At first and second phases, it generates current satisfied to lower 4-bit data. At third phase, it makes 8-bit data current by integrating current which are correspond to upper 4-bit and lower 4-bit data. We can express the output current of the circuit as equation (1)

$$I_{output} = \sum_{i=4}^{8} 2^{i-4} D_i \cdot I_{ref} + \frac{1}{4} \times \frac{1}{4} \times \left(\sum_{i=1}^{4} 2^{i-1} D_i \cdot I_{ref} \right) = \sum_{i=1}^{8} 2^{i-1} D_i \cdot I'_{ref} \quad (1)$$

In detail, at the first phase, current from the current source is divided into the current ratio of 3 to 1 and the current is sampled by N0 when the size of N1 is three times larger than N0. At this time input current from the current source is generated according to the digital data. For example, if the lower 4-bit digital data is “1110” then generated current in current source stage can be obtained by equation (2)

$$2^3 D_4 \cdot I_{ref} + 2^2 D_3 \cdot I_{ref} + 2^1 D_2 \cdot I_{ref} + 2^0 D_1 \cdot I_{ref}) = 14 \cdot I_{ref} \quad (2)$$

And sampled current in N0 can be calculated from equation (3)

$$\frac{1}{4} \times (14 \cdot I_{ref}) = \frac{14}{4} \cdot I_{ref} \quad (3)$$

As same as the first phase, at the second phase, current is divided into ratio of 3 to 1 and the current is sampled by P0 which is three times smaller than P1. Now, the sampled current in P0 sampled current which correspond to the lower 4-bit data is obtained by equation (4)

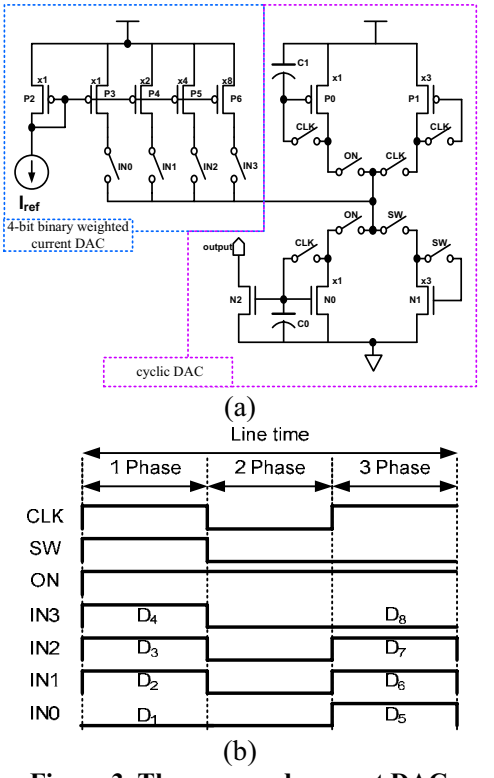


Figure 3. The proposed current DAC. (a) Schematic diagram and (b) Timing diagram when input data is ‘11100111’

$$\frac{1}{4} \times \left(\frac{14}{4} \cdot I_{ref} \right) = \frac{14}{16} \cdot I_{ref} \quad (4)$$

At third phase, N0 superposes current composed with lower 4-bit from P0 and upper 4-bit from current source. If the upper 4-bit digital data is “0111, then generated current in current source stage is as expressed in (5)

$$2^3 D_8 \cdot I_{ref} + 2^2 D_7 \cdot I_{ref} + 2^1 D_6 \cdot I_{ref} + 2^0 D_5 \cdot I_{ref}) = 7 \cdot I_{ref} \quad (5)$$

And sampled current in N0 is calculated from equation (6)

$$\frac{14}{16} \cdot I_{ref} + 7 \cdot I_{ref} = \frac{126}{16} \cdot I_{ref} \quad (6)$$

3. Simulation results

We verified the performance of the proposed DAC by simulations using HSPICE [5]. Figure 4 shows simulation results of the proposed circuit, and the waveforms represents the current levels flowing through N0 and P0. At the first, second and third phases, sampled currents in N0,

P0, and N0 are 56.7nA, 14.1nA, ad 12.6uA, respectively. This result is same as the value which is calculated by equation (6).

Figure 5 shows simulation results of the error ratio of the proposed circuit. Figure 5(a) and Figure 5(b) exhibit performances of differential nonlinearity (DNL) and integral nonlinearity (INL), respectively. As shown in Figure 5(a) and Figure 5(b), all the errors are less than 0.5 LSB. We used clock-feedthrough compensation technique for minimizing the switching error [4]. The proposed current DAC is simulated under the condition of 5V supply voltage, and 2.4 inch/qVGA resolution format. In this case, 8-bit gray scale expression from 10nA to 2.56μA of current level is assumed. They are summarized in Table 1.

Table 1. proposed circuit simulation condition

Item	Value
Pixel Number	300 x RGB x 240
Resolution	qVGA
Driving voltage	5 V
Gray scale	8-bit
Line time	17.36μs
Output current range	10nA ~ 2.56μA

4. Conclusion

We proposed an area efficient 8-bit current DAC which can be applied to current driving AMOLEDs for mobile applications. The proposed DAC has about 70% smaller area than that of the typical binary weighted current DAC. We improved previous current cyclic DAC to overcome sampling time by reducing the number of repetition phases so that it can display 8-bit gray scale image [3]. Consequently, the proposed circuit can sample low level current. Also the circuit has simple operation. Therefore, it reduces a number of interconnection lines, from 8 to 6.

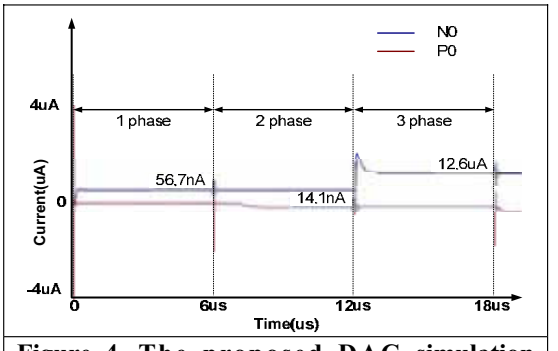
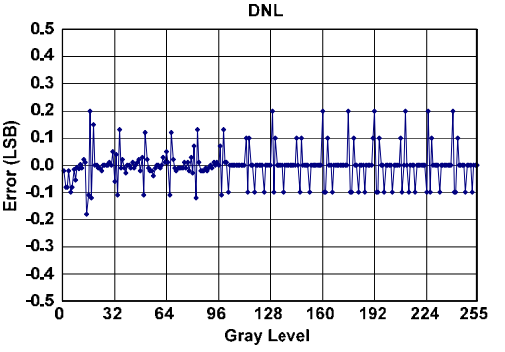
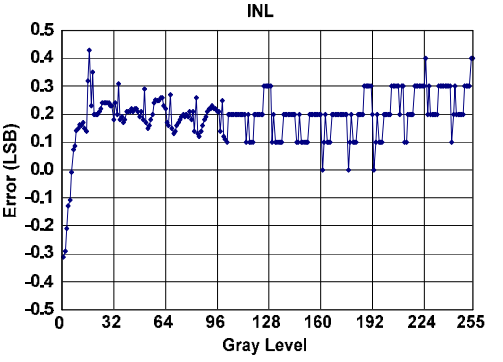


Figure 4. The proposed DAC simulation result when input data is '11100111'



(a)



(b)

Figure 5. The error ratio of the proposed Current DAC (a) DNL and (b) INL

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