Poly-Si TFT on Metal Foil for 5.6-inch UTL (ultra-thin and light) AMOLED

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Abstract

The optimization of poly-Si TFT process on metal foil for UTL AMOLED was systematically investigated. The improvement in device performance of poly-Si TFT on metal foil was achieved by optimizing the dopant activation condition and gate dielectric structure. Hence, the world first flexible full color 5.6-inch AMOLED with top emission mode on poly-Si TFT stainless steel foil is demonstrated.

1. Objectives and Background

Recently, the market's demand for the slim mobile display with high resolution and full color is rapidly increasing. Because active-matrix organic light emitting diodes (AMOLED) display has the advantages such as fast response time and wide viewing angle as well as thin thickness compared to AMLCD, it is expected that AMOLED display will come into the mobile market such as hand-held phone and personal digital assistance (PDA) in near future.

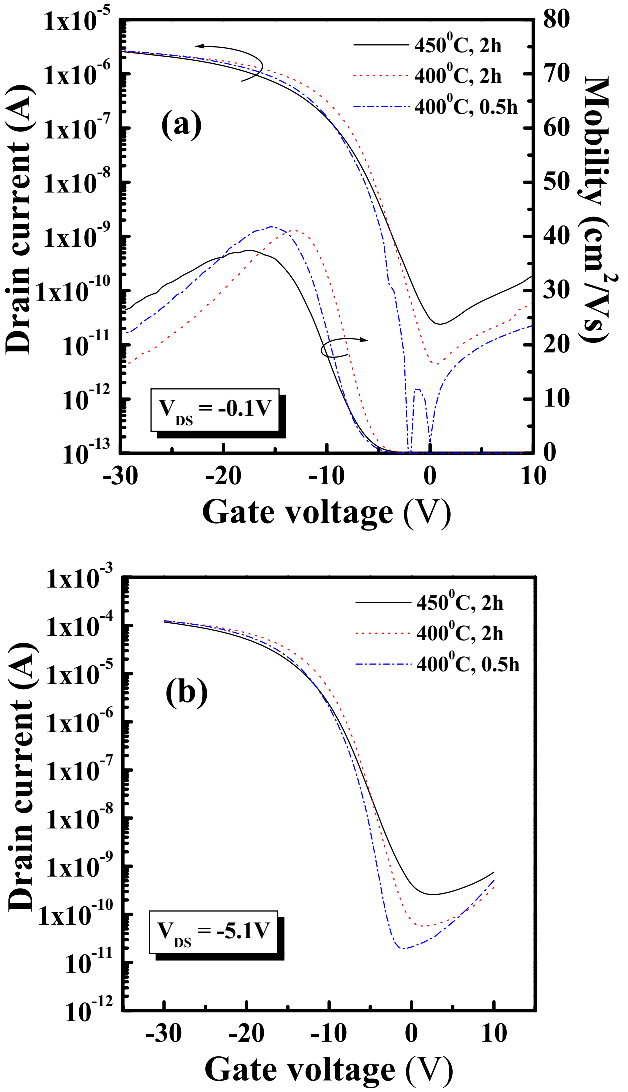

Figure 1. The transfer characteristics of a poly-Si TFT (W/L=10/10μm) on metal foil for various activation conditions at (a) V_{DS}=-0.1V and (b) V_{DS}=-5.1V. The calculated channel mobility curves are also inserted in Fig 1(a).

However, AMOLED display on glass substrate is still thick, fragile and heavy. To overcome these drawbacks, it is essential to replace the conventional glass substrate with new material substrates such as plastic and stainless steel, which can be much thinner, lighter and unbreakable. Much effort has been focused on plastic substrates [1,2]. However, it is very difficult to obtain the TFT array with good device performance because only low temperature process below approximately 150°C is acceptable in the case of plastic substrates. In addition, the dimensional instability during the fabrication process and handling issue of plastic substrates should be considered. On the other hand, a stainless steel foil has the excellent diffusion barrier against moisture and oxygen, thus, there is no permeation problem, which is prerequisite for the flexible AMOLED. There are the reasons why

AMOLED display on stainless steel is promising for the next generation mobile application. In this paper, we demonstrated the world first 5.6” flexible AMOLED on stainless steel foil using LPTS TFT array. Much effort is focused on the optimization of p-channel poly-Si TFT on metal foil.

2. Results

The amorphous Si film with 50-nm-thickness was grown on buffer layer/stainless steel by low-pressure chemical vapor deposition (LPCVD) at 450°C. The flow rate of Si_2H_6 and SiH_4, which were used as source gases for Si film, were 50 sccm and 50 sccm, respectively. Crystallization of a-Si film was done by excimer laser crystallization (ELC) technique. After patterning the poly-Si active layer by using photolithography and dry etching, a gate dielectric and gate metal (a 200-nm-thick MoW) were deposited by PECVD at the substrate temperature of 310°C and sputtering at room temperature, respectively. After gate metal was patterned by wet etching, the ion shower doping for the ohmic contact of source and drain was performed within an energy range of 70 ~ 85 keV using B_2H_6 plasma. Before activating the boron dopant by using furnace, the interlayer stack of a 100-nm-thick SiN_x and 300-nm-thick SiO_2 was deposited by PECVD. Then, the contact hole was defined by photolithography and following dry and wet etching. The source, drain, and data line (a 500-nm-thick MoW) were finally patterned.

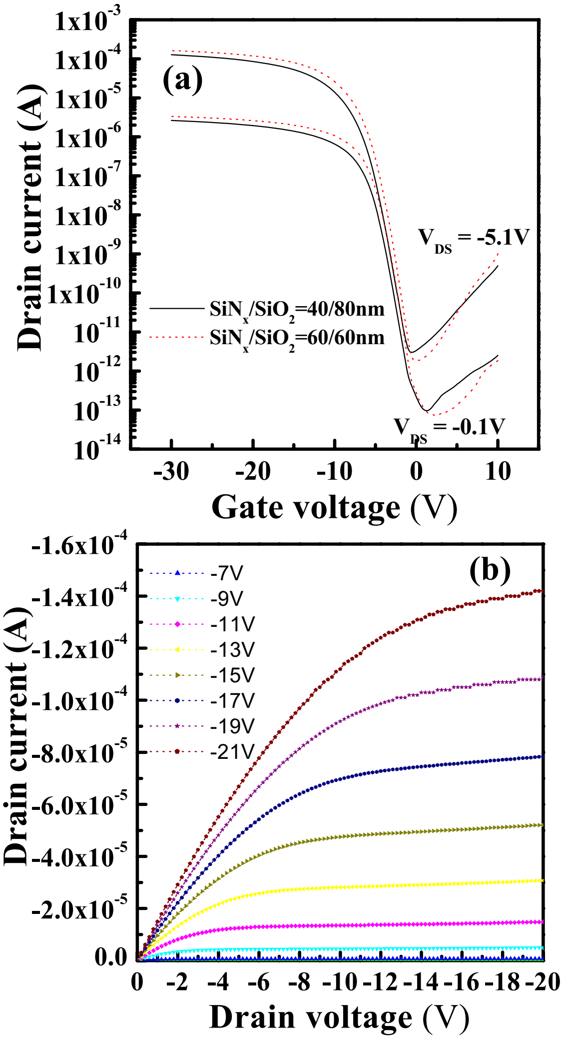

Figure 2. (a) The transfer characteristics of a poly-Si TFT (W/L=10/10μm) on metal foil with SiNx/SiO_2 = 40/80nm and SiN_x/SiO_2 = 60/60nm as a gate dielectric. (b) The output curves of a poly-Si TFT with the bi-layer gate structure of SiN_x/SiO_2 = 60/60nm (for V_{GS} = -7V ~ -21V in 2V steps).

Figure 1(a) shows the representative transfer characteristics of poly-Si TFT with the single gate dielectric (100-nm-thick SiO_2) and W/L = 10/10 um on stainless steel foil as a function of the dopant activation condition. The field effect mobility (u_{FE}) by the trans-conductance at low drain voltage (V_{DS} < -1V) is determined by

$$\mu_{FE} = Lg_m / WC_iV_{DS}$$

where C_i and g_m are the capacitance of the gate insulator and trans-conductance, respectively. The p-channel conduction with the channel mobility of 37.4cm^2/Vs and threshold voltage of -3.7V was observed for poly-Si TFT at the activation condition of 450C, 2hr. It is noted that the influence of the activation conditions on the average mobility and threshold voltage of poly-Si TFT is statistically negligible within the significance level of 0.05. In contrast, the S-factor and off current of poly-Si TFT were dramatically improved with decreasing the thermal budget. Hence, at the activation condition of 400°C and 0.5hr, the S-factor of 1.08 V/dec and off-current of 2.51×10^{-13} (A/μm) for the p-channel poly-Si TFT were obtained while the poly-Si TFT at the activation condition of 450°C and 2hr had the S-factor of 2.19 V/dec and off-current of 1.26×10^{-12} (A/μm). Presumably, the impurity out-diffusion of metal components such as Cr, Fe and Ni etc. through the buffer layer into poly-Si active layer is responsible for this result. Diffusion length can be estimated as following,

$$x_0 \approx \sqrt{D_o \exp(-\frac{E^*}{kT})t}$$

where D_o, E^*, T and t are the diffusion coefficient, activation energy, temperature and time, respectively. It is tentatively assumed that the diffusion length of metal components through the buffer layer decreases with the decreasing activation temperature and time, which resulted in the lower off-current and improved S-factor.

Next, in order to improve the pMOS interface properties, the gate stack of SiN_x and SiO_2 instead of the single SiO_2 (100nm) gate dielectric was adopted for poly-Si TFT on stainless steel foil. The representative transfer characteristics were shown in Fig. 2(a). The solid and dot line were taken from the poly-Si TFT with the gate dielectric of SiN_x/SiO_2 = 40/80nm and 60/60nm, respectively. The S-factor of poly-Si TFT with the gate stack of SiN_x (40nm) and SiO_2 (80nm) was enhanced to 0.81 V/dec, compared to that (1.08 V/dec) of poly-Si TFT with singe SiO_2 (100nm) dielectric. Furthermore, it should be noted that poly-Si TFT with the gate stack of SiN_x (60nm) and SiO_2 (60nm) showed the better interface (S-factor = 0.72 V/dec) and transport characteristics (μ_{FE} = 52.0 cm^2/Vs) without degrading the off-current of poly-Si TFT. It can be understood that the enhanced hydrogen passivation of the interface traps and/or grain boundary defects of polycrystalline Si constitutes the reason for the improvement in TFT device performance. These improvements in the mobility, S-factor and off-current of poly-Si TFT with bi-layer gate (SiN_x/SiO_2=60/60nm) were reflected by the excellent output characteristics exhibiting the clear pinch-off and current saturation, as shown in Fig. 2(b).

The top emission structure was developed because the stainless steel foil is not transparent to visible light. The top emission structure has the reflective anode, organic layers and transparent cathode on the TFT backplane. The reflective anode (ITO/AlNd) has a high reflectivity of 90%. OLED device structure consisted of hole injection layer (HIL), hole transport layer (HTL), RGB emitting layer (EML), hole blocking layer (HBL), electron injection layer (EIL), and transparent cathode. The phosphorescent materials for Red and Green, and fluorescent materials for Blue were used as an emitting material, respectively. Especially, the novel OLED structure using a blue common layer (BCL) was adopted on TFT backplane. That is, after Red and Green colors were sequentially patterned by evaporating the small molecule using the shadow mask on TFT backplane, the BCL was directly deposited without the show mask. It should be emphasized that this technique provides the advantage of eliminating the blue pattering step.

Multilayer, thin-film encapsulation, which is comprised of the organic and inorganic composite barrier layers, was performed by Vitex System Inc.

Items	**Specification**
Diagonal size	5.6 inch
Number of pixels	160×3×350
Resolution	66 ppi
Panel size	77×375 μm^2
Aperture ratio	60%
Pixel element	2 TFT + 1 CAP
Gray	64 gray (262,144 colors)
Scan driver	PMOS-only integration
EL luminescence	150 cd/m^2
Color coordinate	Red (0.69, 0.30) Green (0.26, 0.70) Blue (0.14, 0.07)

Table 1. The specification of a 5.6 inch top emission AMOLED on stainless steel foil.

The specification of the 5.6-inch AMOLED prototype is summarized in Table 1. The developed display has the pixel number of (160×RGB×350) at the resolution of 66ppi. Its sub-pixel pitch is the 125×375μm^2 with the aperture ratio of 60% and pixel element of 2 transistors and 1capacitor. Figure 3 shows a display image of UTL AMOLED being bent. The overall thickness of AMOLED was less than 0.15mm, which is the world's thinnest flexible AMOLED. We note that the display image without any distortion was observed even though it was bent to the curvature of approximately 7cm.,

Figure 3. The display image of the 5.6 inch top emission AMOLED display on stainless steel foil emission AMOLED on stainless steel foil.

3. Impact

Several research groups have reported the fabrication of Si TFT arrays on metal foil as a display backplane [3-6]. Serikawa et al. have focused on the integration of poly Si TFT on stainless steel substrate [4], and Xie et al. reported EL deposition on metal foil as a test cell [7]. LG Phillips Inc. has reported 10.1-inch black/white electrophoretic display on stainless steel foil, which was driven by amorphous Si TFT and E-ink microcapsules in FPD 2005. We have already reported 4.1-inch mono color AMOLED display on stainless steel foil in SID 2005 [8]. Most research groups have showed TFT array performance on metal foil and mono color display. In contrast with previous works, our flexible AMOLED display can show high-speed full color video, and has only the thickness of 150um and 1/4 weight compared with the same size of AMLCD.

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