High Resolution Electrodes Fabrication for OTFT Array by using Microcontact Printing and Room Temperature Process

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Abstract

The flexible organic thin film transistor (OTFT) array to use as a switching device for an organic light emitting diode (OLED) was designed and fabricated in the microcontact printing and room temperature process. The gate, source, and drain electrode patterns of OTFT were fabricated by microcontact printing process. The OTFT array with dielectric layer and organic active semiconductor layer formed at room temperature or at a temperature lower than 40 ℃. The microcontact printing process using SAM and PDMS stamp made it possible to fabricate OTFT arrays with channel lengths down to even submicron size, and reduced the fabrication process by 10 steps compared with photolithography. Since the process was done in room temperature, there was no pattern shrinkage, transformation, and bending problem appeared. Also, it was possible to improve electric field mobility, to decrease contact resistance, to increase close packing of molecules by SAM, and to reduce threshold voltage by using a big dielectric.

1. Introduction

The organic thin film transistors (OTFTs) can be fabricated using a number of different device structures. In general, OTFTs are comprised of four components: gate electrode, gate dielectric, organic active semiconductor layer, and source and drain contacts. OTFTs can be fabricated either with a horizontal device structure, where the electric current flow is perpendicular to the substrate and in which the channel length is defined by lithographic resolution, or with a vertical device structure, where the current flow is perpendicular to the substrate and in which the channel length is determined by film thickness [1, 2]. The OTFT is required to reduce the operating voltage less than 5V for active organic EL, a plastic chip for inventory tags and smart cards. We have two approach methods such as decrease the channel length and the thickness of gate dielectric [3]. When fabricating OTFT arrays on flexible substrate, substrates warpage, surface roughness, and layer-by-layer registration methods should be considered, and the several problems such as optical characteristics deterioration caused by exceeding the maximum process temperature, incoherent pattern arrangement by shrinkage and transformation, and loosening of the adhesion between organic and inorganic materials should be solved to improve the performance [4, 5].

This study was design and fabrication an OTFT array which can be fabricated through a microcontact printing and a room temperature process and will be used as a switching device of an OLED. The gate, source, and drain electrode patterns of OTFT were fabricated by microcontact printing process which is high-resolution lithography technology using poly(dimethylsiloxane)(PDMS) stamp. The OTFT array with dielectric layer and organic active semiconductor layers formed at room temperature or at a temperature lower than 40℃. During the OTFT fabricating process, in order to keep the flatness, we used dry film photoresist(DFR) as adhesion layer and glass substrate as rigid layer adhered to PEN layer.

For a design in pursuit of efficiency improvement and commercialization of an OTFT, it is necessary to investigate high heat resistance, high coplanarity and high optical transmittance technology, and large-area substrate design and to develop new materials on source/drain, gate electrodes, insulators, organic semiconductor layer, plastic substrates, and so on; also necessary is a manufacturing method considering On/Off ratio, mobility, etc [6].

2. Design and Fabrication Process

The microcontact printing is a promising technology for replicating nano/micro patterns of a master by fabricating a PDMS stamp, staining patterns on the PDMS stamp by functional ink, transferring onto a

substrate and conducting an etching process or vapor deposition process [7, 8]. The gate, source, and drain electrode patterns of OTFT were fabricated through the microcontact printing process using as a mask PDMS stamp on which an SAM used as an etching mask was applied selectively. As high-resolution and large-area OTFT arrays could be fabricated by using the microcontact printing process. The mask size is 5 x 5 x 0.9 inch, and the channel length is 5um where the line width and the pattern space are different. Figure 1 shows the mask for conducting a patterning experiment on 16 pattern zones on a 4 inch silicon wafer, and a device structures were designed and manufactured on the 20 x 20mm zone located respectively.

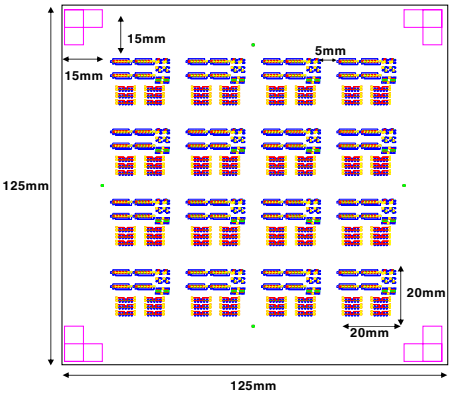

Figure 1. Geometry of designed pattern form for 5" size OTFT array mask

As to the plastic substrates for fabricating OTFT arrays, we used polyethylenenaphthalate(PEN, Teijin Dupont Films) which thickness was 200um, and surface roughness was 0.6nm, coefficient of thermal expansion(CTE) was 20ppm/℃ at 200℃, thermal shrinkage was 0.02%(150℃X30min.), and so they had excellent thermal safety characteristics, H_2O permeability was low and O_2 permeability was also low, the chemically resistant characteristics against acid and alkaline was excellent, and Young's Modulus was high, and so they had high strength characteristics. The parylene-C was used as organic insulation layer. The parylene-C is a primary dielectric, exhibiting a very low dissipation factor, high dielectric strength, and a dielectric constant invariant with frequency. The parylene-C of which dielectric strength is 5600(DC volts/mil short time), sheet resistance is 1014 (Ω, 23 ℃, 50%), and dielectric constant is 3.15(60Hz), has the excellent conductive characteristics [9, 10].

On the PEN substrate, we deposited 10nm of Cr as adhesion layer and 100nm of Au as etching layer using e-beam deposition device maintained below 50 ℃ inside the chamber, and inked hexadecanethiols(HDT) SAM solution up to PDMS stamp, transferred into PEN substrates through registration contact printing, and formed single layers. Also, selectively etched Au using TFA/GE-8148 solution and fabricated conductive gate electrode. On the fabricated gate electrode, we deposited parylene-C with high permittivity at room temperature using deposition device and formed organic dielectric, and then coated with positive photoresist in 1um thickness under the condition of maintaining OFPR at 3000RPM for 20 seconds and prebaked at 90℃ for 30minutes. Then carried out lithography process using gate mask and developed with NMD solution for 80 seconds. Selectively etched patterned organic insulation film using O_2 plasma at 130W of RF power for 10 minutes. And photoresist removed in MS solution at 70℃ for 8 minutes. On the parylene-C organic insulation layer, we made 1um of channel length and carried out patterning of source and drain metal electrodes using microcontact printing process, inked HDT SAM solution up to PDMS stamp transferred into PEN substrates through registration contact printing, and formed electrodes. On the source and drain metal electrodes, we deposited 10nm of Cr as adhesion layer and 100nm of Au as etching layer. And on the contact electrodes, we deposited 100nm of pentacene as organic active semiconductor layer using e-beam deposition method. On the pentacene organic semiconductor, we formed passivation layer by depositing 1um of parylene. Then coated with positive photoresist in 3um thickness under the condition of maintaining AZ PR at 3000RPM for 20 seconds and prebaked at 90℃ for 30minutes. And

carried out patterning using lithography process using pentacene mask and fabricated organic semiconductor by means of eliminating unnecessary parts using O_2 plasma. Figure 2 show fabrication process of OTFT by using microcontact printing.

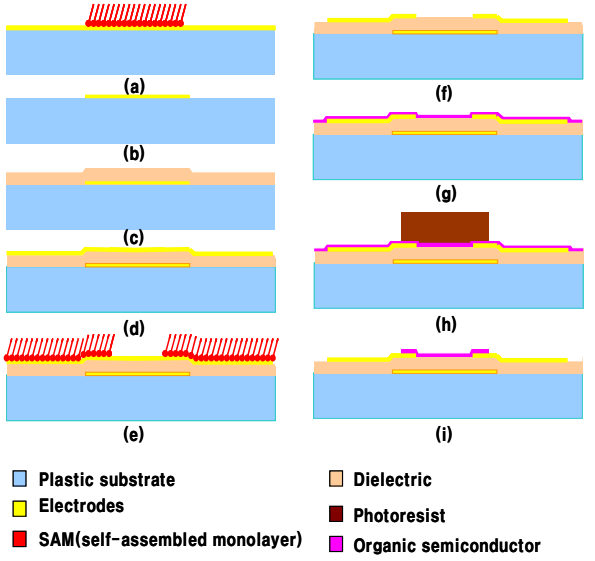

Figure 2. Fabrication process of OTFT using uCP (a) Inked SAM solution on Au deposited plastic substrate, (b) fabricated gate electrode, (c) deposited and patterned dielectric, (d) Au deposition, (e) Inked SAM solution for contact electrodes, (f) fabricated source and drain electrode, (g) deposited organic semiconductor, (h) patterned organic semiconductor, and (i) fabricated organic semiconductor

3. Experiment and Results

As to the plastic substrates for fabricating OTFT, Au/Cr thin films were deposited on a PEN plastic substrate at a temperature lower than 40℃ inside a chamber and a conductive gate electrode was fabricated using the microcontact printing process. The parylene-C was deposited on the fabricated gate electrode to create an insulator layer and the patterned organic dielectric was etched by oxygen plasma. The source and drain metal electrodes were patterned and fabricated on an insulator layer using microcontact printing process. The pentacene which is an organic active semiconductor layer was deposited on a contact electrode through a room temperature. Figure 3 show deposition process of parylene-C dielectric at room temperature. During the OTFT fabricating process, in order to keep the flatness, we used dry film photoresist(DFR) as adhesion layer and glass substrate as rigid layer adhered to PEN layer. Then put the glass substrate on the hot plate maintained at 60℃, cut the DFR film in proper size, and adhered closely flattening out using roller and then, adhered PEN film to the glass substrate without passivation layer on the hot plate.

An exclusive device was used to enable room temperature process of conductive electrode, insulator, and organic semiconductor layers, so that it was possible to minimize CTE caused by shrinkage and extension due to temperature of a plastic substrate and to provide better alignment in the patterning process. Besides, since there was no substrate deformation, it was possible to prevent optical property degradation. The parylene-C was used as a gate insulator to reduce threshold voltage. An OTFT array was fabricated through the microcontact printing process using SAM and PDMS stamp to prevent a leakage current from lowering the efficiency of a device and reduce degradation and to enable micro/nanopattern fabrication of OTFT. When fabricating OTFT using microcontact printing process, since there was no need for photolithography device, and photo process, we could reduce the procedure by 10 steps or more. Since the fabrication process was done in low temperature, there was no pattern transformation and bending problem appeared. Figure 5 was SEM image of OTFT fabrication with line width of the pattern was 10um, pattern channel length was 5um using microcontact printing and room temperature process.

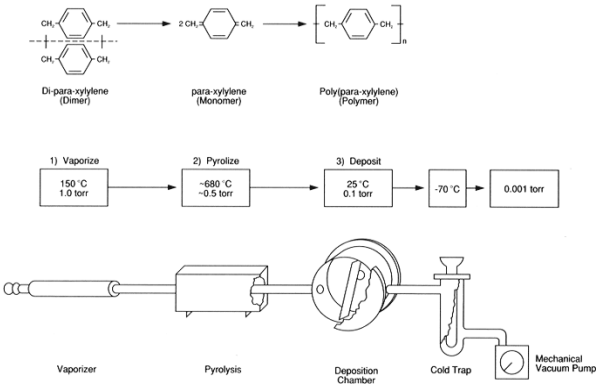

Figure 3. Deposition concept and process of parylene-C dielectric at room temperature

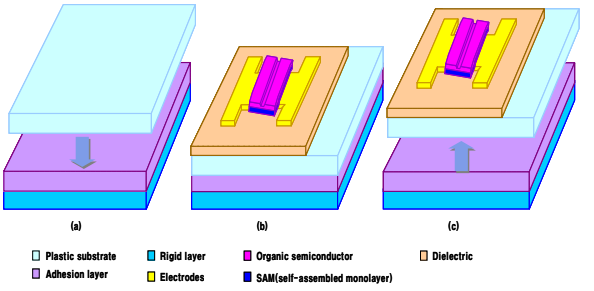

Figure 4. Mount method for maintain flatness during process

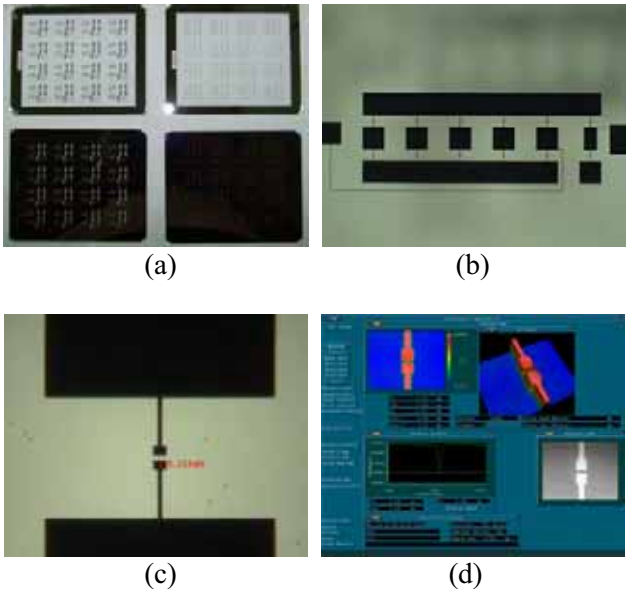

Figure 5. Results of OTFT Array fabrication: (a) fabricated 5" size quartz mask, (b) patterned source/drain, and gate electrode on PEN substrate, (c) channel length (source/drain) of 5um, and (d) 3D profiler image of printed electrode.

4. Conclusion

The microcontact printing process using SAM and PDMS stamp made it possible to fabricate OTFT arrays with channel lengths down to even submicron size, and reduced the fabrication process by 10 steps compared with photolithography, there was no need for exposure, develop, and remove process. Since the process was done in room temperature, there was no pattern shrinkage, transformation, and bending problem appeared. The flexible OTFT array was fabricated through the microcontact printing and room temperature process, so that it was possible to improve electric field mobility, to decrease contact resistance, to increase close packing of molecules by SAM, and to reduce threshold voltage by using a big dielectric.

5. Acknowledgements

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