A 2” QCIF Flexible OTFT driven AM-OLED Display

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Abstract
The flexible 2-inch AMOLED with 176 x 144 pixels has been demonstrated using top emission OLED driven by organic thin film transistors (OTFTs). For the development of AMOLED display on plastic substrate, we have developed several integration and unit process technologies. Through the optimization of the process based on plastic substrate, OTFT backplane with 2 transistors and 1 capacitor in a pixel has been fabricated and integrated with top emission OLED. The active addressing by OTFT driving circuit has been achieved and green light with 15 cd/m^2 at 15V has been observed.

1. Introduction
In recent years there has been growing interest in the field of organic thin film transistors (OTFTs) on plastic for organic electronics such as smart cards, low cost identification (ID) tags, and flexible displays. [1] OTFT offer advantages compared to traditional field-effect transistors, like mechanical flexibility and weight reduction. [2] Also, many researchers have been interested in OTFT-OLED display on plastic substrates. Among the switching devices for OLED (organic light emitting device), OTFT is promising for its compatibility with low temperature processes on plastic substrates. While plastic substrates are flexible, thin, light weight, tough, and so on, their poor dimensional and thermal stability leads to many difficulties in integrating processes for electrical devices. Moreover, although flexible OTFT-OLED has advantage of low temperature process, it needs many new materials and processes to realize truly low temperature process. [3-5]

Up to now, many researchers have tried to fabricate an OTFT for AM display on the plastic substrates. [6-8] Most of them have been manufactured through a simple patterning process using shadow masks to avoid many troublesome lithography processes, which can not be applied to high resolution display.

In this article, we report a flexible QCIF(Quarter Common Intermediate Format) AM-OLED display on plastic substrates. We use conventional integration processes such as photolithographic process, wet cleaning process, via etching process for OTFT backplane rather than shadow mask process. Although the conventional integration process led to several problems to overcome such as de-lamination in metal contact process, surface morphological change of pentacene, leakage in interlayer, we have successfully fabricated the OTFT backplane by using several new techniques developed by us. Top emission OLED has been integrated with the OTFT backplane by using shadow mask process. Finally, thin film encapsulation with parylene and AlO_x layers resulted in a 2-inch QCIF flexible OTFT driven OLED display. In this presentation, the detailed integration process and some factors affected on the properties of OTFT-OLED display will be discussed.

2. Integration processes of OTFT-OLED
The plastic substrates used in the work was a 120 μm-thick PC(polycarbonate) sheet supplied by Tejin Co. The pentacene TFTs were fabricated using a bottom-contact structure. Cr/Al/Cr deposited by sputtering and Ti/Au by e-beam evaporation were used for the gate and the source/drain metals, respectively.. An organic gate insulator, J1(polyacrylate derivatives) was deposited onto the patterned gate metal by spin coating. The gate patterns were planarized by the spin-coated J1 at a thickness about 300 nm. We use Au as source/drain and it is patterned by a fast lift-off method using a lift-off machine designed by ourselves. Pentacene is deposited by PCOVD (pressure control organic vapor deposition) method which can be applied to large substrate. AlO_x as an etch stopper of gate dielectric in active etching is deposited by ALD (atomic layer deposition) method. and parylene as a protecting layer after active layer deposition is deposited by CVD. This passivation layer protects pentacene against any

attack with the solvents used for the photolithographic process. Pentacene and parylene layer are patterned by ECR(electron cyclotron resonance) etcher using only O_2 gas. For interlayer insulation and planarization, PIL is spin-coated by a thickness of 3 µm. ZWD (a kind of PR) of 0.7 µm is used as an edge passivation of OLED pixel. For the OLED, we treat the surface of anode with O_2 plasma and then deposit NPB and Alq3 by a thickness of 600Å using a thermal evaporator. And LiF/Al/Ag is used as cathode electrode. Thin film passivation was performed with AlO_x by ALD.

3. Results

The full integration process for OTFT-OLED display on plastic substrate is carried out with a conventional semiconductor process. In general, thermal processes cause curls and thermal expansion/shrinkage of plastic substrates, which becomes the origin of the peeling or cracking of the deposited layers on them. Therefore, it is very difficult to handle the plastic substrate itself because of flexibility. So, we prepared the PC substrates by laminating on Si wafers by SASD(strong attach & soft detach : strongly adhesive in edge region and weakly adhesive in inner-side region) method, which was reliable enough for our processes and also easily detachable the substrates from the wafer.

To overcome the lithographical misalignment occurring from the thermal and dimensional instability of plastic substrate during typical processes, we used the particular method called by TDE (Time-Delay Expose), in which the exposure after the bake of PR was delayed in some time which is adjusted according to the expansion of the substrate at each process. The misalignment of 5µm per inch may be permitted on PC using this method. Figure 1 shows the alignment between the successive layers by this photolithographic process.

A gate metal of multi-layers with Cr/Al/Cr (10 nm /100 nm /10 nm) was deposited by sputter. Organic insulator of J1 was used as a gate dielectrics by spin coating. This material has good dielectric properties with the low curing temperature(≤150℃), smooth surface roughness (~3Å), low leakage current(<10^{-9}A/cm^2 @40V), and reasonable dielectric properties(dielectric constant K=3.7 @1MHz, dielectric loss is 0.03 @1 MHz).

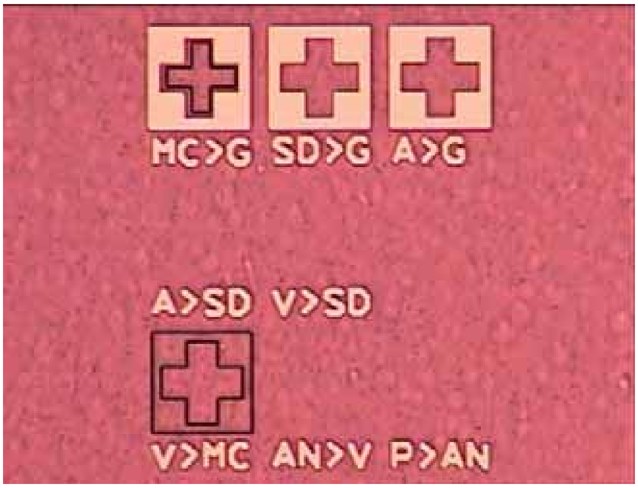

Figure 1. An alignment status between the successive layers using the TDE method.

Ti/Au(5 nm /80 nm) is used for source and drain electrode deposited by e-beam evaporation.

Pentacene as organic semiconductor was deposited using PCOVD method, which can be applied to large deposition area with high quality thin film. This technology is suitable to obtain high quality organic thin film due to the possibility of the working pressure variation with various carrier gases during deposition compared to the conventional evaporation method at fixed pressure. Parylene deposited by CVD was used for a passivation layer. And then, an active layer patterning was performed by conventional photolithographic process. Without patterning of the active layer, there occurs many problems such as cross talk, reduction of I_{on}/I_{off}, and failure of metal contact due to the poor adhesion of pentacene film to its underlayer. Figure 2 shows a SEM image of a metal contact by the peeling problem without the active layer patterning.

We carried out the active layer patterning by oxygen plasma. After the parylene and pentacene layers were successively etched, the photoresist as an etch mask was removed by normal PR(photoresistor) removing solvent. Although the PR strip process causes to reduce the mobility of our organic transistors, there were not any other problems such as the cracks or peeling of the pentacene layer. Fortunately, the on/off (I_{on}/I_{off}) ratio was greatly increased from 10^4 to 10^7 as a result of active layer patterning .

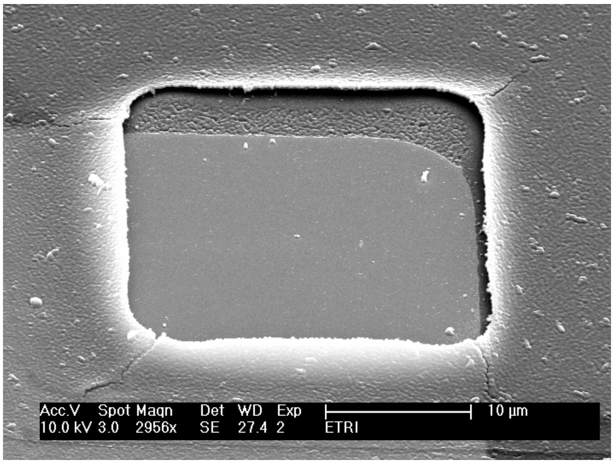

Figure. 2. Peeling phenomena of metal contact

Anode metal of Cr/Al/Cr was deposited by sputter and patterned by wet process. Edge passivation of anode with PR was performed by conventional photolithography.

Figure 3 shows the transfer (a) and output (b) characteristics of OTFT at various gate voltages. Width/length of OTFT is 1000/10 µm. The mobility, $I_{on}/I_{off,}$ and V_{th} of OTFT on PC is 0.24 cm^2/Vs, 10^4, and about 14 V, respectively.

Figure 4 shows the mobility change of OTFT depending on the integration(A : after deposition of active layer, B : after passivation of active layer, C : after patterning of activation layer, D : after deposition of 2nd passivation layer, E : after etching of via, F : after interlayer insulator deposition, G : after anode patterning). At first, the mobility of OTFT was decreased by more than 80% through process. However, we optimized the processes so that the mobility decreased only 50% after whole process.

Top emission OLED has been fabricated on Cr/Al/Cr anode. To remove any contaminants on anode surface, O2 plasma treatment was performed. The organic layers of NPB (600Å) and Alq3 (600Å) were deposited by thermal evaporation with shadow mask. LiF(10Å) / Al((20Å) / Ag (200Å) as a semi-transparent cathode, NPB layer as a buffer layer, and IZO layer as a passivation layer were sequentially deposited by evaporation in the same vacuum chamber.

Encapsulation of OTFT-OLED panel was performed with Parylene and AlO_x layers fabricated by CVD and ALD methods, respectively.

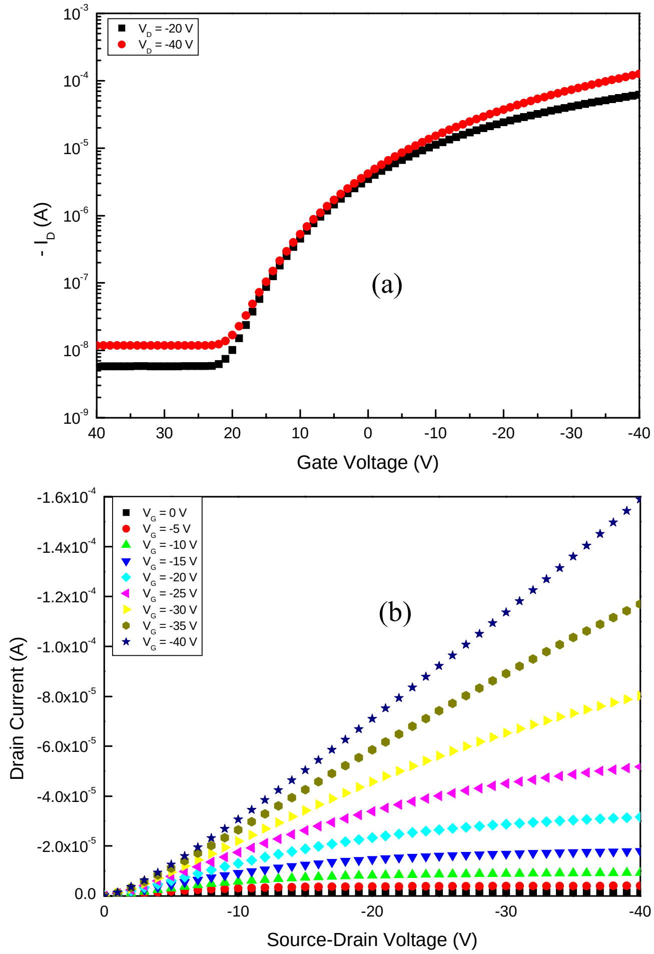

Figure 3. (a) Transfer characteristic and (b) output characteristic of OTFT on PC plastic substrate.

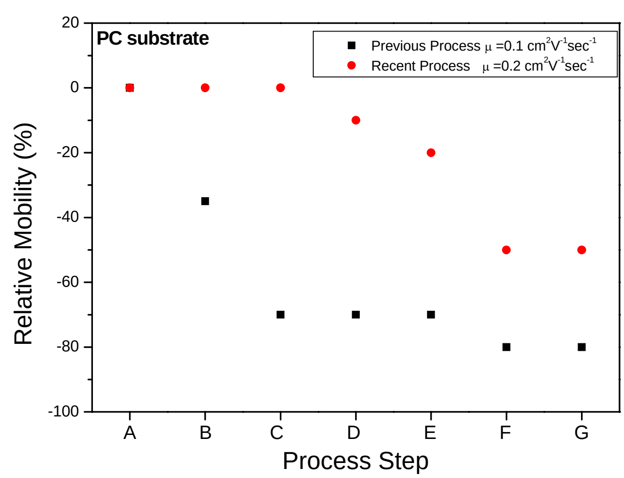

Figure 4. Change of the OTFT mobility on the process step.

Figure 5 shows the pixel picture of the AM-OLED backplane with two-transistor and one-capacitor per pixel on plastic substrates. A pixel pitch is 240x240 µm and an aperture ratio is 20 %. The W/L of driving and switching transistors was 100 µm/ 10 µm and 120 µm/ 10 µm, respectively.

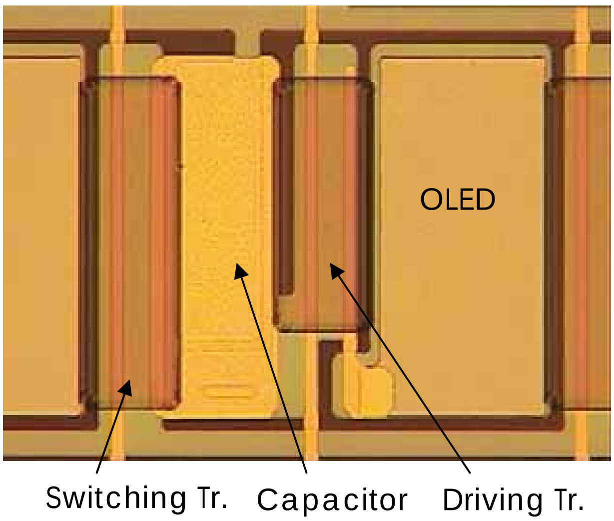

Figure 5. Optical microscope picture of the pixel in an AMOLED backplane on plastic substrate.

Figure 6 shows a flexible QCIF OTFT array which was detached from Si substrate. Figure 7 shows flexible 2-inch QCIF OTFT-OLED panel. The brightness of panel is about 15 cd/m^2 at 15V and we have confirmed that the panel is actively addressed by OTFT driving circuit.

3. Conclusion

We have developed a flexible 2-inch flexible AMOLED display with OTFT backplane using the petacene active layer and the top emission OLED. The problems encountered during the integration of OTFT-OLED on plastic substrates have been figured out by using the techniques developed by us. Therefore, we have succeeded in development of OTFT backplane on on plastic substrate using a low temperature process compatible with a conventional semiconductor process. Although the process needs more improvement for practical applications, we believe that these technologies are expected to bring up a new area of flexible AMOLED.

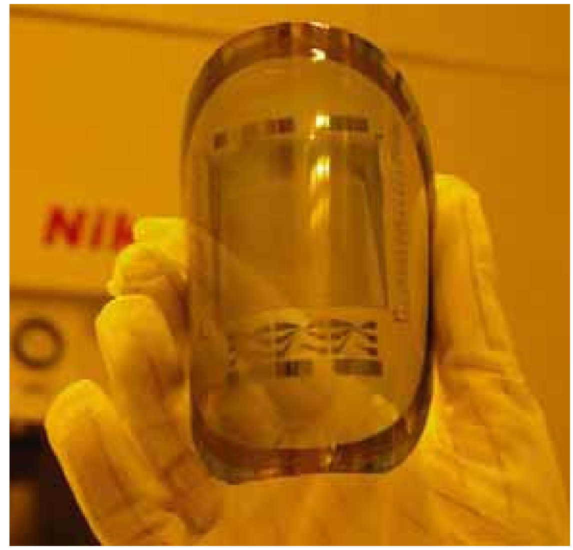

Figure 6. A flexible QCIF OTFT array on PC substrate.

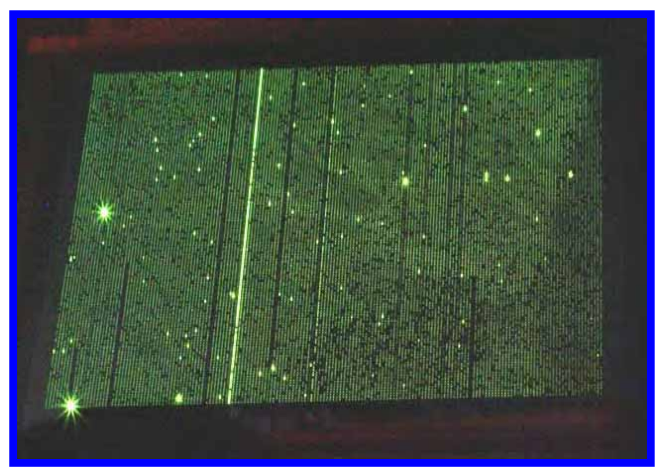

Figure 7. A flexible QCIF OTFT-OLED.

4. Acknowledgements

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