LAYOUT VERIFICATION METHOD FOR DESIGNING AND MANUFACTURING OF LCOS/AM OLED MICRODISPLAY BACKPLANES

A.G. Smirnov , S.N. Koukharenko, S.V. Volk, A.M. Zayats
Belarusian State University of Informatics and Radioelectronics (BSUIR)
P. Brovki Str. 6, 220027 Minsk, Republic of Belarus
Tel. +375-17-2938858, fax: +375-17-2938486, smirnov@gw.bsuir.unibel.by

Abstract

In this presentation we will describe two core elements, which combination gives a new approach to layout verification; they are a computational algorithm for modeling of photolithographical processes and a method for physical layout verification that uses output contours of that algorithm. Utilization of this approach allows to improve the quality of LCOS/AM OLED backplanes physical verification, because it considers discrepancies between mask features and printed contours on a wafer.

Key words: microdisplay, LCOS / OLED backplane, layout verification method

I. Introduction

Ongoing reduction of critical dimensions of a LCOS/OLED silicon backplate elements significantly outpaces industry's adoption of new technological processes that use radiation of a smaller wavelength. As a result, chip manufacturers are forced to operate in a so called 'subwavelength area'. It creates a number of problems, with main issue being deviation of shapes of manufactured elements on a silicon wafer from the 'ideal' shapes shown on a layout. Layout designers are no longer allowed to neglect these deviations of real elements from their representations in the layout database and have to take into account distortions, created by technological manufacturing processes. Coherency between a mask layout and a printed image is broken, and consequently methods of creation and verification of layouts need to be revisited.

This paper presents an algorithm for numerical modeling of contours produced by a subwavelength lithography during LCOS/OLED backplane manufacturing and dwells on an application of the algorithm for layout physical verification.

II. Algorithm of Modeling of Lithographic Processes

Manufacturing process of modern LCOS/OLED IC microchips using optical subwavelength lithography is affected by a number of different factors, leading to distortion of shapes of manufactured elements from their topological description. Optical factors, etching, diffusion and implantation factors, as well as chemical-mechanical polishing are among them [1, 2]. The main factor causing distortions in a subwavelength lithography is an impact of optical discrepancies, produced by an optical system due to finite size of a pupil of a projection optical system and, as a consequence, limited resolution of an optical system as a whole [3]. Pure impact of optical factors is a good first-order approximation for a lithography manufacturing process [2, 4] therefore this article considers only an algorithm for computation of an aerial image produced by optical system on the surface of a photoresist.

In this case, the most suitable method of computations is usage of special branch of optics, named Fourier-optics [5, 6]. The most important distinguishing feature of a modern optical photolithography from the modeling point of view is usage of partially-coherent illumination [2, 3] and this fact is reflected in the algorithm, described below.

The scheme of an optical system of a typical VLSI manufacturing tool is shown on Fig. 1. Its mathematical model consists of the following elements (x and y denote canonical spatial coordinates [3, 6], while f and g denote coordinates in frequency domain):

1. Illumination source, described by two-dimensional brightness distribution function S (x, y).

2. Photomask, described by two-dimensional complex transmission function O (x, y). Transmission function characterizes amplitude and phase of the planar wave in each point right behind the photomask plane.
3. A pupil of a projection optical system is described by complex function P (f, g), which describes impact of the pupil on a spectrum of a passing wave. From a point of view of the Fourier-optics, the pupil performs filtering of high-frequency components in the frequency spectrum domain of an optical image [5, 6].
4. Physical parameters, describing a lithographical tool: radiation wavelength, numerical aperture of the projection optical system lens, aberrations, etc.

Algorithm for computation of light intensity distribution (called and aerial image) on a surface of a photoresist is based on the source integration method [6] and consists of the following steps:
1. A spectrum of spatial waves in a plane just after photomask is computed. The spectrum is computed using analytical formulas, which allow computation of a complex matrix U (f, g),

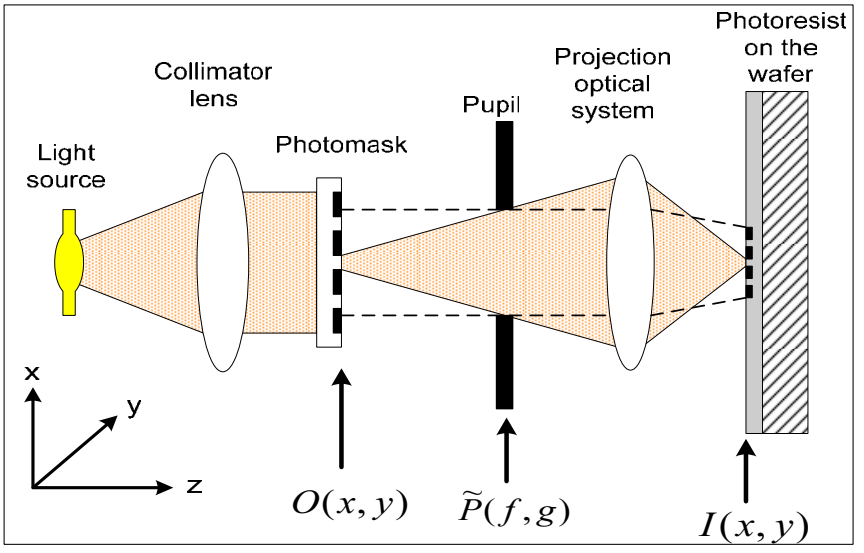

Figure 1: Scheme of the optical system

describing an image spectrum. This calculation uses coordinates of polygons of a photomask that are specified by a transmission function O (x, y).

2. A spectrum of spatial waves in a plane right behind a pupil of a projection system is computed. The spectrum is computed by multiplying each element of the U (f, g) matrix, obtained in the previous step, by a corresponding value of a function P (f, g), shifted according to a point of an illumination source being currently considered.

3. Coherent image from a single illumination source point is obtained by inverse Fourier transform of the matrix computed in step 2. As we do all computations on a computer, it is reasonable to use an algorithm of Fast Fourier Transform (FFT) for that purpose [6].

4. Amplitudes of coherent images from each point of the illumination source, obtained by repeating steps 2-3 with different source points, are summed with weights determined by brightness distribution function S, to obtain final light intensity distribution ('aerial image') on a surface of the photoresist using partially-coherent illumination.

Result of the computation is a matrix of real numbers I (x, y), describing distribution of light intensity on a plane of a wafer. It can be visualized or passed as an input to another mathematical model, which would build geometrical contours describing printed features. After that these

contours can be viewed by the user or used for layout verification. The latter application is described in the following section.

III. Layout Verification Based on Lithography Modeling

Computational algorithms of modeling of lithographical processes can greatly augment traditional approaches to layout physical verification. Traditional DRC-based verification methods can be viewed as a set of geometric rules a layout must comply with. However, these methods give only a binary "yes-or-no" answer and don't take into consideration variation of process parameters and contour distortions.

A method has been developed by the authors that could accompany conventional methods of physical layout verification by removing its main drawback – conventional methods doesn't account distortions of layout features, which may occur after manufacturing using a submicron lithography [7].

The idea of the new approach is to substitute a large and complex modern DRC rule deck, which considers only shapes of original mask primitives, with a set of much simpler rules, which consider shapes of manufactured contours. These shapes are obtained using the computational model of lithography described above. Mask layout and parameters of optical system are passed to this model as an input, and the model outputs shapes of contours after lithography.

Verification is achieved by building a set of rules, which obtained contours should comply with in order a layout to be manufacturable. For example, there should be a "no bridging" rule and a rule of minimal allowed distance between two printed contours, etc. For each rule we elaborated an algorithm that performs a series of elementary geometrical operations (union, intersection, distance measurement, grow, shrink etc). Each algorithm creates a set of error markers and puts it over a layout for the user to inspect and fix. These markers highlight places where corresponding rules were violated (see Fig. 2). An approach like that is usually called a method of manufacturing rules checking (MRC). The paper [8] dwells upon this approach.

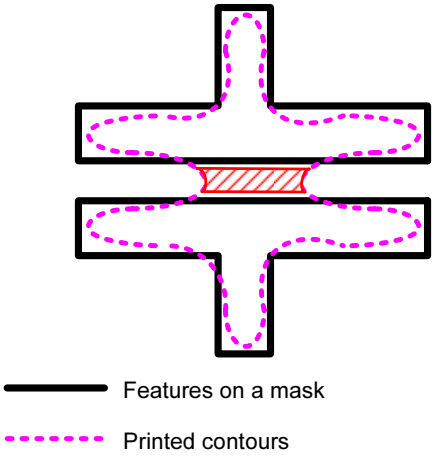

Figure 2: A result of a "Bridging" MRC rule calculation. Dashed error marker shows a place where a bridge between two originally independent features appears

However, each run of a computational model shows printed contours only for a particular combination of input parameters (defocus, exposure, etc). In real manufacturing environment it's unable to fix parameters exactly, and they tend to vary around central values. In other words, instead of an exact value of a parameter only a certain probability law can be evolved (typically, a Gaussian one). Due to a high sensitivity of modern lithographical equipment, these slight variations may cause significant differences in printed contour shape. And since a lithographical model accepts only exact parameter values, a same piece of a layout needs to be modeled several times,

varying input parameters of a model. In turn, each model run is time-consuming, what leads to a significant loss of time spent on iterative checks or makes the user to reduce size of an area under check. Apparently, there is a need to change MRC in a way that it could consider parameter variations and at the same time remain as time-cheap as possible.

The proposed method tries to get as many information from every single model run as possible by determining the extreme distortions of printed contours with a given probability and applying conventional MRC rules to distorted contours. If a design remains MRC-clear after that, it means that it is tolerant to variations of technological parameters with the selected probability. This probability reflects overall yield.

All contour distortions can be split into two types – systematical and random ones. Systematical distortions affect contour shapes across the whole layout in a similar way. For example, stepper defocus produces this type of distortions. In circuit design it can be accounted for as a variation of some parameter value equally across all devices and structures of a design. Random deviations occur spatially across a chip on a non-uniform basis. They may be caused by local defects of a mask, random particles, etc. Both types of distortions have stochastic nature and can be described by certain probability laws that should be provided by foundry and correspond to a certain manufacturing process and equipment.

We illustrate our approach on an example of contour sizing defect. Size mismatch of a printed contour against its expected size is a sum of systematic and random components:

$$\Delta x = S_x + R_x,$$

where S_x is contribution of systematic factors, R_x is contribution of random factors. These factors take place independently.

Systematic sizing defects may occur mainly because of defocus or dosage variation. These dependencies are generally non-linear and are determined implicitly by the computational model, but we can deduce them by approximation. In order to do that, a special test layout should be prepared and passed as an input to lithographical model. The layout consists of a one large square. Since an image on a wafer is produced by mask features within a limited radius, a length of square edge should be no less than twice that radius. The radius is usually equal to five wave lengths [9], hence edges should have length at least ten wavelengths. The test layout is then modeled under different conditions and contour sizing measured exactly in the middle of the edge. As a result, a dependency of sizing from a selected factor may be deduced. An equation $S_x = F(D)$ may be deduced where S_x is a systematic sizing error and D is a selected disturbing factor. Sizing along different axes may be evaluated separately in case of an asymmetric illuminator.

Since a law of distribution of the selected factor and a law of random sizing error distribution should be known from the foundry and a dependency between sizing and the factor was approximated, it is possible to deduce a law of distribution of a total sizing error via composition. Usually, both laws of distribution are Gaussian $N(m_D, \sigma_D)$ and $N(m_R, \sigma_R)$. If S_x is approximated linearly as $S_x = aD + b$, then the resulting distribution will be also a Gaussian one:

$$N(am_D + m_R + b, \sqrt{(|a|\sigma_D)^2 + \sigma_R^2})$$

This formula may be more complex if a dependency of systematic sizing is approximated with a polynomial of a higher power or when several of lithographical parameters are considered, but this does not change the whole approach. Using the resulting formula, a range $[x_a, x_b]$ can be determined, in which sizing error falls with a given probability (say, 90%, 95% and 99%).

Now we can perform computational modeling of a piece of a layout with nominal values of parameters and obtain a set of "nominal" contours. Then a check of all MRC rules should be performed twice – the first time after over-sizing the nominal contours by x_b and the second time after under-sizing them by x_a. As a result, new defects can be discovered that don't occur at nominal values of parameters but are probable in real manufacturing environment (see Fig. 3).

If a layout is MRC-clear even with under- and oversized contours, it means that the design is robust and tolerant to sizing errors with a selected probability. Apparently, the closer probability is to 100%, the wider the range $[xa, xb]$ is, thus the more conservative a design requires to be. The

layout on the previous figure exhibits low tolerance to contour sizing errors due to variation of manufacturing parameters and should be re-designed.

However, it should be noted that even after all these actions are performed, it cannot be guaranteed that all manufacturing defects were discovered, because different layouts and different pieces within the same layout have different sensitivity to defocus variations. Therefore, the proposed method needs calibration each time it is applied to a new piece of a layout. The method can be calibrated by selecting a test layout and places of measurement of deviations. For example, if contour deviation would be measured not in the middle of edges but along corner bisector, then the *[xa, xb]* range may become wider, and therefore there will be more places of rule violations.

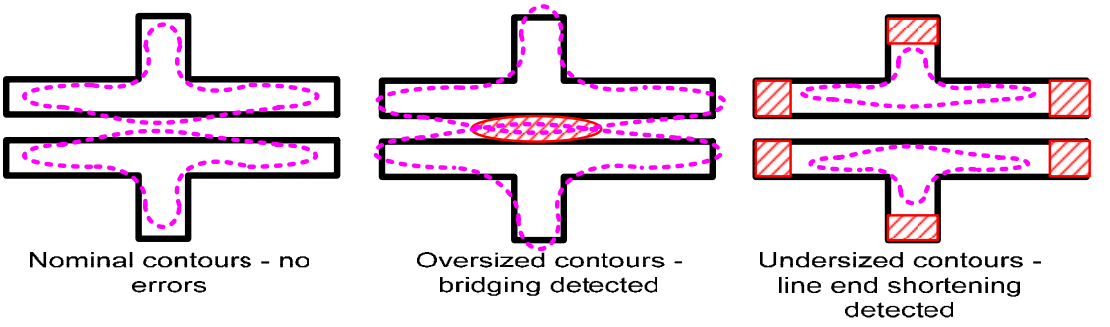

Figure 3: Resizing of "nominal" contours may help discovering hidden MRC errors.

The described approach may also be used to detect places on a layout that exhibit high sensitivity to parameter variations. To do that, we need to compare contours obtained with the described scheme of over- and undersizing against contours obtained with direct computational modeling with manufacturing parameters set to deviated values directly. If a discrepancy between two contours is large then a corresponding mask feature exhibits a larger or smaller sensitivity towards varying of a selected set of manufacturing parameters than an expected average value.

IV. Conclusion

In this article we have described two core elements, which combination gives a new approach to layout verification; they are a computational algorithm for modeling of lithographical processes and a method for physical layout verification that uses output contours of that algorithm. Utilization of this approach allows improving quality of LCOS/OLED backplanes physical verification, because it considers discrepancies between mask features and printed contours on a wafer.

V. References

[1]. Clein D. CMOS IC Layout: Concepts, Methodologies and Tools. – Elsevier Science & Technology Books, 2000.
[2]. Levinson H. Principles of lithography. – SPIE Press, 2001
[3]. Wong A. Resolution Enhancement Techniques in optical lithography. – SPIE Press, 2001.
[4]. Rai-Choudhury P. (Ed.). Handbook of Microlithography. – SPIE Press, 1997.
[5]. Born M., Wolf E. Principles of Optics.6th ed. – 1997
[6]. Goodman J. Introduction To Fourier Optics. – 2nd ed. – 1996
[7]. Markosian A., Rencher M., "Model-based approach allows design for yield". – eeTimes Online. [http://www.eetimes.com/showArticle.jhtml?articleId=160900827]
[8] Sahouria E., Granik Y., Cobb N., and Toublan O. Full-chip Process simulation for silicon DRC. Technical proceedings of the 2000 International Conference on Modeling and Simulation of Microsystems. [http://www.nsti.org/procs/MSM2000/2].
[9]. Wong A., "Resolution Enhancement Techniques in optical lithography". – SPIE Press, 2001.