Low temperature plasma deposition of microcrystalline silicon films for bottom gate thin film transistors

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Abstract

We review our studies on the growth of microcrystalline silicon films by the standard PECVD technique. In situ spectroscopic ellipsometry studies allow the optimization of the complex film structure with respect to competing aspects of the growth process. Fine tuning the hydrogen flux, the ion energy, and the nature of the species contributing to deposition produces unique films with a fully crystallized interface with silicon nitride. These materials have been successfully incorporated in bottom gate TFTs which present mobility values in the range of 1 to 3 cm^2/V.s, and stable characteristics when submitted to a bias stress. The stability of these TFTs makes them suitable for driver applications in AMLCDs as well as pixel elements in OLED displays.

1. Introduction

Active matrix liquid crystal (AMLCD) displays based on a-Si:H thin film transistors are a fast expanding industry despite some limitations related to the properties of a-Si:H, which result in low field effect mobility and poor stability. To address these issues various approaches have been studied, in particular the use of polycrystalline silicon obtained by annealing a-Si:H at ~ 700 °C (SPC) [1], by excimer laser crystallization [2] or by metal induced lateral crystallization (MILC) [3]. However, in all these approaches homogeneity is a large concern.

Many attempts have been made to directly deposit microcrystalline or polycrystalline silicon by PECVD. Indeed, this a very appealing technique as it allows the production of the films in the same plants which today produce a-Si:H TFTs for AMLCDs. Moreover, very high values of mobility have been achieved in coplanar top gate µc-Si:H TFTs. However, from an industrial perspective, a bottom gate structure would be preferable as it is fully compatible with today's a-SiH TFTs. Although mobility is an important parameter, stability and low off current values are also key issues for practical applications. In this paper we review our recent work on the microcrystalline silicon growth process, in particular from SiF_4-Ar-H_2 mixtures. This gas mixture results in films with large grains, comparable to those produced by SPC at 700°C. Results on bottom gate TFTs with mobility values above 1 cm^2/V.s, excellent stability and ON/OFF ratios of 10^5-10^6 are reported. Moreover, we have achieved materials with mobility values as high as 21 cm²/Vs as deduced from TRMC measurements. This suggests that high mobility TFTs can be achieved with films deposited at low temperature and leads us to discuss the limiting factors in TFT parameters.

2. Experiments

We deposited µc-Si:H films on Corning glass substrates at 200 °C by the dissociation of SiF_4-H_2-Ar gas mixtures in a standard RF glow discharge system. The total gas pressure was fixed at 1.8 Torr and the RF power at 290 mW/cm². The structural properties of the films were studied by UV-Visible spectroscopic ellipsometry measurements. The ellipsometry data were modelled through the use of a Bruggeman Effective Medium Approximation theory (BEMA) [4]. As shown in table 1, the optical model used to describe the films consists of three layers: a surface roughness, a thin subsurface layer and the bulk material. The composition of each layer was characterized by a fraction of small grain polycrystalline silicon (F_{sg}), large grain polycrystalline silicon (F_{lg}), mono-crystalline silicon ($F_{c\text{-}Si}$) and voids (F_v). Raman scattering was used to check the crystalline fraction of the films[5] by decomposing the measured spectra into three Gaussian peaks centred at 520, 500 and 480 cm^{-1}. The first peak is ascribed to crystallites with large grain, the peak around 500 cm^{-1} can be assigned to the contribution from small grains and grain boundaries, while the peak at 480 cm^{-1} represents the amorphous

phase[6]. Transmission electron microscopy was performed on selected samples to support ellipsometry and Raman analysis. The electron mobility in the layers was characterized by time resolved microwave conductivity (TRMC). This technique is based on the change of the reflectivity of the materials in the microwave range due to carriers photogenerated by a 5 ns pulsed Nd:YAG laser at 532nm; the microwaves are generated by a gun diode at 28 GHz. It is important to note that TRMC measures the mobility inside the crystallites, taking into account trapping but not grain boundary barriers [7]. Finally a-SiN:H/µc-Si:H/n+(a-Si:H) stacks were made into bottom gate TFTs.

3. Results and Discussion

We use UV−Visible elliposmetry to characterize the grain size in our films. This is based on the fact that the optical absorption in crystalline silicon shows two prominent structures at 3.4 eV and 4.2 eV, well predicted from its electronic band structure and particularly sensitive to imperfect crystallinity [8]. In the case of polycrystalline silicon, the variations in the energy position of E1 and E2 with crystal size have been predicted both theoretically and experimentally observed [9].

Figure 1 shows the imaginary part of the dielectric function of crystalline silicon, large grain and small grain polycrystalline silicon [10]. One can clearly see that the amplitude of E_1 and E_2 depend on the crystal size, the more ordered is the material the more pronounced are the peaks.

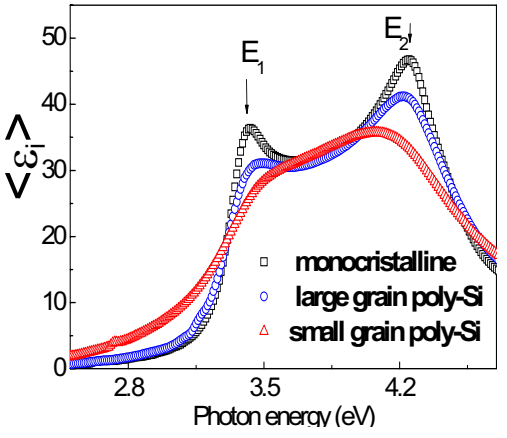

Figure 1. Imaginary part of the dielectric function of crystalline silicon and of large and small grain poly-crystalline silicon.

We compare in Figure 2 a large grain polycrystalline film obtained by SPC with a µc-Si:H directly deposited on glass at 200 °C by PECVD. We can see that the peaks E_1 and E_2 are more intense and pronounced for the films deposited by plasma, which indicates a better crystallinity in spite of the low temperature process.

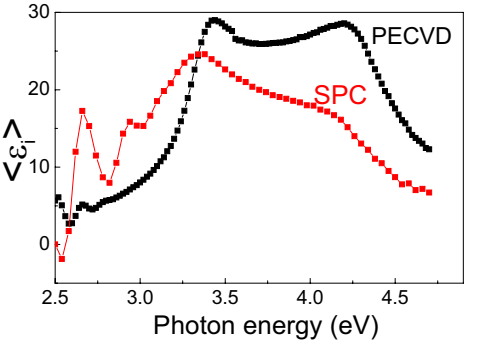

Figure 2. Imaginary part of the pseudo dielectric function of a SPC film and of a film deposited by PECVD.

This is supported by the BEMA modelling of the experimental data as shown in Table 1. We can see that the composition of the bulk of the two materials is similar, with a high fraction of crystalline silicon and small grain polycrystalline silicon. The same applies for the subsurface region; only the surface roughness shows a smaller thickness indicating that PECVD films are smoother.

Table 1. Optical model used to fit the ellipsometry data of SPC and PECVD films.

SPC		PECVD	
5.5nm	F_v =58% F_{lg} = 42%	2.4nm	F_v =37% F_{cSi} = 63%
48.6nm	F_{sg} = 64% $F_{c\text{-}Si}$ = 36%	13.6nm	F_{sg} = 44% $F_{c\text{-}Si}$ = 50%
185nm	F_{sg} = 53% $F_{c\text{-}Si}$ = 47%	559nm	F_{sg} = 51% $F_{c\text{-}Si}$ = 44%
Glass		Glass	

The above results are confirmed by Raman spectra measurements, as shown in Figure 3. Indeed, both materials present a narrow peak at about 518 cm^{-1}, along with a slightly more pronounced shoulder at ~ 500 cm^{-1} for the PECVD film, characteristic of a larger fraction of grain boundaries. In both cases the

crystalline fraction from Raman is about 70%, i.e. smaller than that from ellipsometry as already reported [11].

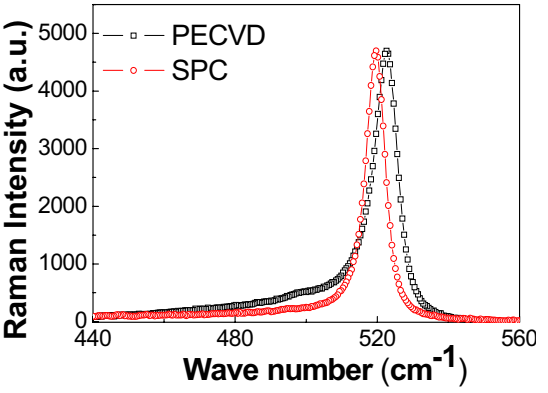

Figure 3. Raman spectra for samples deposited by PECVD and SPC.

The presence of large grains was also checked by transmission electron microscopy. Figure 4 gives an example of a cross section of a film deposited at 200°C for which a columnar structure with large grains is clearly observed. The electron diffraction pattern confirms that the film is polycrystalline

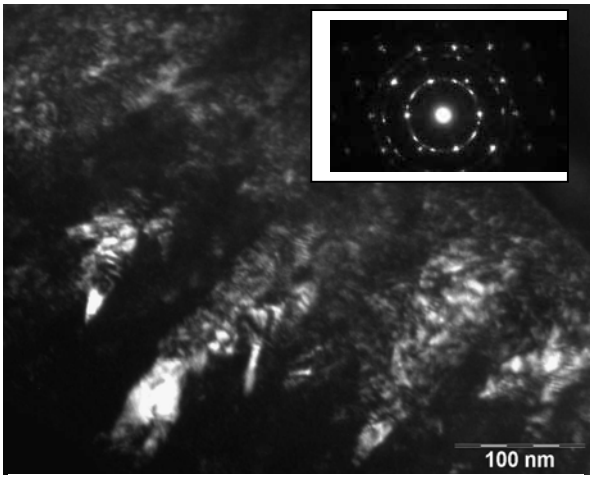

Figure 4. Transmission electron microscopy of a large grain polycrystalline silicon film deposited by PECVD at 200 °C. The electron diffraction patters shown in the inset confirms its polycrystalline nature.

Time resolved microwave conductivity measurements (TRMC) were performed to check if the presence of large grains translates into improved transport properties. This contactless method is based on the change of the reflectivity coefficient of the material in the microwave range when an excess carrier density is generated via a pulsed laser light [12]. The change in the reflectivity is proportional to the product $\mu_{eff}\delta n(t)$, where μ_{eff} is the sum of electron and hole mobility, and $\delta n(t)$ is the excess carriers concentration.

In order to optimize the µc-Si properties we produced numerous sets of samples with varying discharge parameters (RF power, total pressure, inter-electrode distance,…). In Figure 5 we report the effect of the hydrogen flow rate on the film structure and on the electron mobility. We can see that the total crystalline fraction (F_c) of the films deposited from SiF_4-Ar-H_2 mixtures decreases with increasing hydrogen flow rate. More interestingly, the fraction of large grains (F_{LG})in the material has an optimum for a hydrogen flow rate in the range of 1-5 sccm, while it decreases for higher and lower flow rates. Additionally, the electron mobility deduced from TRMC follows the same trend as the fraction of large grains. In particular the sample deposited with 1 sccm of hydrogen shows a mobility of 22 $cm^2/V.s$.

The above materials have also been applied to bottom

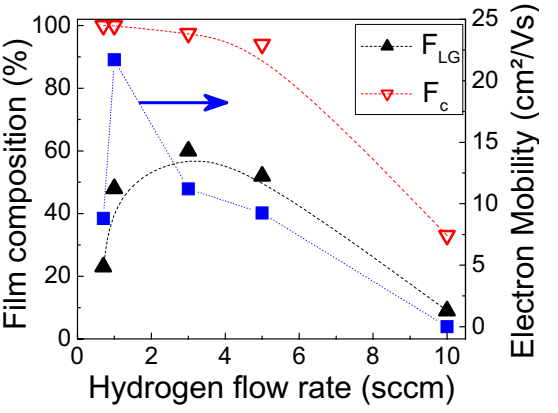

Figure 5. Effect of hydrogen flow rate on the electron mobility (squares) and the film structure: crystalline fraction (F_c) and large grain fraction F_{LG} (triangles).

gate microcrystalline silicon TFTs. Indeed, even though high mobility values have been reported for coplanar top gate TFTs based on microcrystalline silicon [13 , 14], stability, low off current and a

mobility higher than that of a-Si:H are all key aspects. Moreover, a bottom gate structure as used in a-Si:H TFTs is also preferable. However, bottom gate TFTs are more challenging as it is well known that microcrystalline silicon growth is substrate dependent [15] and that the material properties improve with film thickness [16]. The challenge therefore is to achieve a high crystalline fraction in thin films and in particular a fully crystallized interface with the dielectric. In previous studies we have shown that this can be achieved by various deposition methods [17]. As an example Figure 6 shows the transfer characteristics and threshold voltage shift during electrical stress of a bottom gate TFT produced at 200°C from hydrogen dilution of silane. The 500 nm a-SiN dielectric layer was deposited in the same reactor at 250 °C. The semiconductor layers consisted of a 137 nm thick and fully crystallized film with 38% of large grains, followed by 45 nm of n+(a-Si:H) layer as a contact for source and drain. For this device w = 200 µm and L = 10 µm.

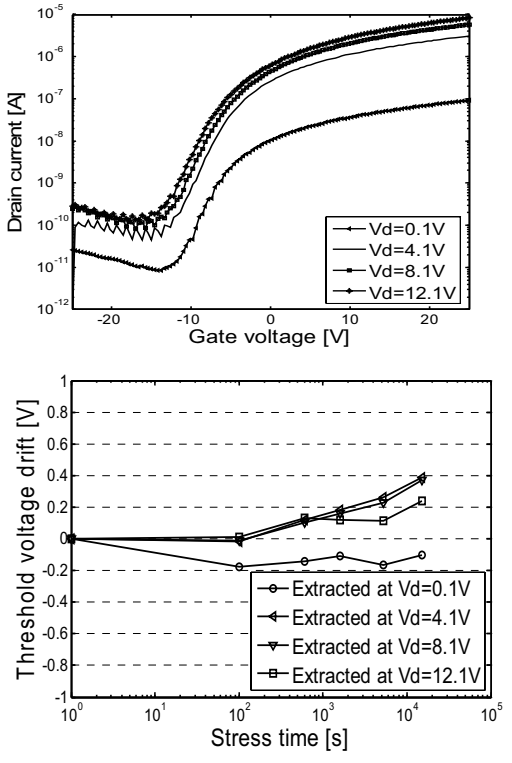

Figure 6. Transfer characteristics and threshold voltage shift as a function of stressing time for a bottom gate µc-Si TFT. Note the excellent stability of V_T.

The threshold voltage and mobility values for this device were 1 V and 1 $cm^2/V.s$ respectively. Moreover, as shown in Figure 6, this device demonstrated a excellent stabilty when stressed at 30°C with a 30 V gate voltage and various values of the drain voltage. We think that this material offers clear advantages with respect to a-Si:H TFTs for AMLCD displays and even more for AMOLEDs, where stability is a key issue. Of course, one would like to achieve higher mobilities and the material studies reported above clearly show that there is room for improvement. In particular, µc-Si films produced from SiF_4-Ar-H_2 displaying large grains and high mobility values hold thus the promise for an improved mobility.

3. Conclusion

We have summarized our studies on microcrystalline silicon deposition by PECVD at 200 °C for application in bottom gate TFTs. The TFT results show that indeed µc-Si is a strong candidate with respect to a-Si:H, in particular because of its excellent stability and capability of higher mobility values. Moreover we have shown that large grain material having electron mobility values as high as 22 $cm^2/V.s$ and a structure similar to SPC films can be produced from SiF_4-Ar-H_2 mixtures.

4. Acknowledgements

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