# A Method to Predict the Performance of a-Si TFT device

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## Abstract

*The driving-current degradation of a-Si:H thin-film transistor(TFT) device has been analyzed for the first time. A method to analyze the performance of TFT circuits is presented, which is different from the conventional one by threshold voltage shift method. It can be also used to evaluate the performance of gate driver on array (GOA) circuit, which is integrated in a 12.1" WXGA (1280*3*800) TFT-LCD panel.*

## 1. Introduction

The integration of drivers and panel not only saves the cost of driver ICs, but also makes the LCD modules very compact. Poly-silicon TFT is widely used to integrate driver circuits and pixels on a single panel because of its high mobility and superior stability. However, an additional process for the crystallization of a-Si:H is needed.

Recently, a-Si:H TFT was popularly used to integrate gate driver circuit on the glass (GOA) for TFT-LCD panel, since it can reduce the total cost of driver IC and simplify the bonding process. Moreover, the fabrication of GOA was compatible with the current a-Si:H TFT process. In many literatures, the method to predict the lifetime of a-Si:H TFT was performed by the stress-time and stress-voltage dependence of the threshold voltage shift ($\Delta V_{TH}$ ), which was based on the stretched-exponential equation to explain the $V_{TH}$ shift, as shown in Eq. (1) [1-3].

$$\Delta V_{TH} = (V_G - V_{T0})\left\{1 - \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right\} \qquad (1)$$

where $\tau$ is some characteristic extractable time constant, and $\beta$ is the stretched-exponential exponent which is temperature dependent.

However, it cannot really predict the real performance of TFTs circuit, since the duty cycle of a TFT operated in the circuit is much higher than that of a TFT typically used in real pixel about 5% to 10%, resulting in the huge drop in the ON current of the TFT more seriously [4].

In this paper, a method to predict the ON-current degradation of a-Si:H TFT for the analysis of the gate driver circuit performance is presented for the first time. Using the proposed method, the measured ON-current degradation of a-Si:H appears to completely agree with the fitting result given by the expression of the stress-time and stress-temperature dependence of the ON-current degradation.

## 2. Experiment

Figure 1 shows the top view of the inverted-staggered a-Si:H TFT structure fabricated by Back-Channel-Etching (BCE) process and the channel width (W)/length(L) of the TFT device is 1000μm /6μm. The sample prepared for the bias-temperature stress was baked for 2 hours at $200^0$Cto eliminate the meta-stable characteristics.

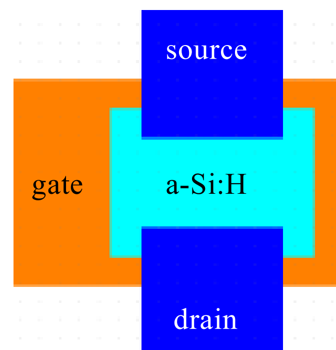



Fig. 1 A symmetric TFT layout design.

The electrical characteristics of TFTs were measured by using an HP-4156B semiconductor parameter analyzer. For the bias-stress experiments, a pulsed bias voltage with a duty-cycle of 50% sweeping from –10V to 23V was applied to the gate electrode of a TFT and a steady-state bias voltage of – 10V was symmetrically applied to the source and

drain electrode of the TFT. All of the samples were measured at the various substrate temperatures ranging from 45$^0$C to 70$^0$C.

## 3. Result and Discussion

Gate driver circuit is composed of many TFTs which are designed to different geometric structures and operated at different bias-stress conditions. However, TFTs with different bias-stress conditions have very different transfer characteristics ($I_D$-$V_G$). So far as the GOA circuits are concerned, the pull-down device is the key component of driver circuit and plays the role to discharge circuit node. It indicates that the discharge ability of the pull-down TFT device is strongly related to driving ability of driver circuits.

In addition, the operation voltage of TFTs will influence the performance of driver circuits. Although the low mobility of a-Si:H TFT leads to the fall of driving ability, applying high driving voltage in circuit or using a-Si:H TFT with large W/L ratio can achieve the required operation current. High driving voltage provides a high driving current but it will induce the threshold voltage shift seriously due to the metastable characteristic of a-Si:H TFT. The method using $V_{TH}$ shift method to predict the performance of real circuits would be not accurate exactly. Figure 2 shows the ON current degradation and the $V_{TH}$ shift of a-Si:H TFTs under bias-temperature-stress conditions with different stress time. While the increase of stress time results in the increase of the $V_{TH}$ shift, the ON current can maintain on the top value of limitation current under the same driving voltage of TFTs.

It is helpful to define the ON current characteristics of TFT to observe the degradation of ON current and driving voltage capability of the device. Most devices of GOA circuit were operated in the saturation region, according to the Eq. (2), the current equation of saturation region before and after bias stress could be shown as following, corresponding to Eq. (2) and Eq. (3):

$$I = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{GS} - V_{T0})^2 = K(V_{GS} - V_{T0})^2 \quad (2)$$

$$I' = K[V_{GS} - (V_{T0} - \Delta V_T)]^2 \quad (3)$$

where $I$ and $I'$ were the ON current before and after bias stress respectively, $K$ is a constant. Expanding Eq. (3) and substituting Eq. (1) and Eq. (2) into Eq. (3), the result is listed in Eq. (4):

$$\frac{I'}{I} = \Delta I = \exp\left[-2\left(\frac{t}{\tau}\right)^{\beta}\right] \quad (4)$$

where β is as a power-law index, and τ is related to the substrate temperature. Thus, the ON current degradation resulted from the bias-temperature stress can be described by an exponential equation with time dependence.

Figure 3 is the plot of the ON current characteristic of a-Si TFT at the temperature of 45$^0$C to 70$^0$C after a long time AC bias stress. The dot point is the measured data and the solid line is the fitting data using Eq. (4). The measured data shows that as the temperature and stress time increase, the ON current drops more seriously. When the ON current is degraded to 17% of its initial value, the stress time at the temperature of 45$^O$C, 60$^O$C and 70$^O$C is 120hr, 36hr and 22hr, respectively. According to Eq. (4), we have obtained a well-fitting line curve in complete agreement with the measured data, where the value of fitting parameter β is about 0.483 and the value of τ falls from 160 to 28 with respect to the rise of the substrate temperature, as shown in Fig. 4.

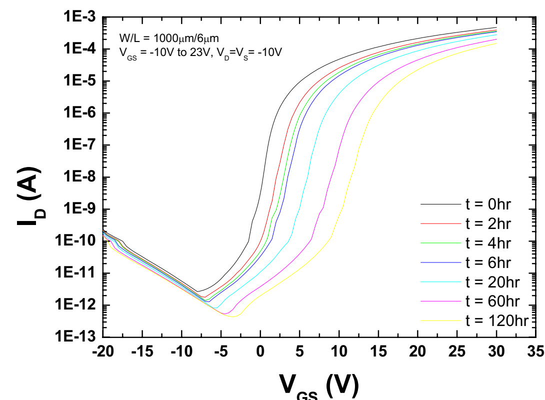



Fig.2 Degradation of a-Si TFTs with different stress time conditions.

If the limitation of the current for the pull-down device is 1*10$^{-7}$ Amp, the operation time of the pull-down device can be estimated to 2773 hours for operating at 45$^O$C. However, the duty ratio of the key pull-down device is not always 50%. Thus, the

lifetime of the pull-down device for real operation should be expected longer than the predicted one.

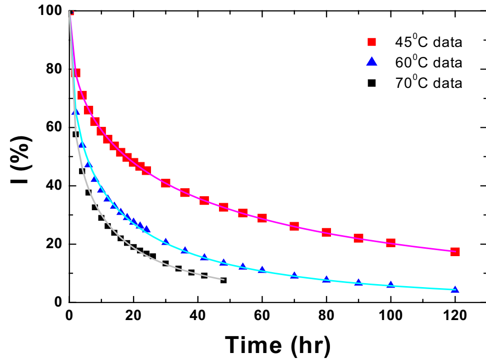
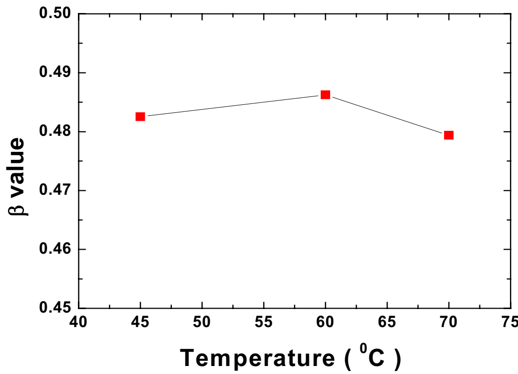
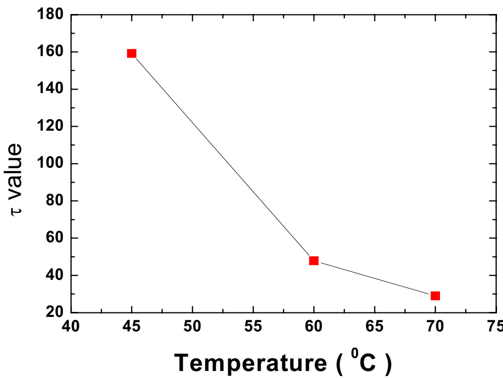



Fig.3 The ON current degradation of a-Si TFTs with driving voltage $V_{GS}$=23V under different substrate conditions; symbols: measurement data, solid line: exponential equation give by Eq. (4).




(a)




(b)

Fig. 4 The β and τ value with different substrate temperature condition: (a) the β value, and (b) the τ value.

## 4. Panel Implementation

Figure 5 shows that 12.1" WXGA (1280*3*800) TFT-LCD panel with the integrated gate driver has been successfully developed by us [5]. The a-Si:H TFT gate driver consisting of 800 stages of shift registers was integrated on one side of the panel. At the same time, pixel TFTs were fabricated by the normal 5-Mask process without any additional process. Figure 6 shows that the gate driver circuit is still possessed of a good and stable output pulse even after the bias stress of 62 hours at 80°C.

Fig. 5 12.1" TFT-LCD panel with a-Si gate driver integration panel

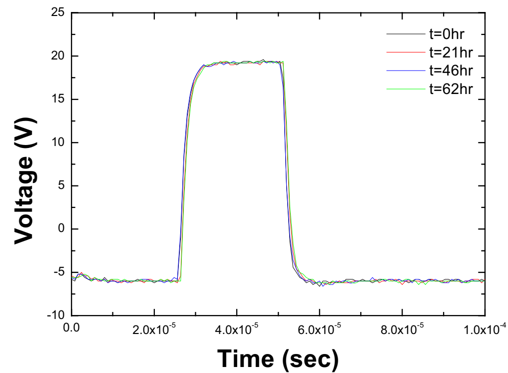



Fig. 6 The output pulse of ate driver circuit after 62 hours at 80°C stress.

## 5. Summary

We have presented a method to predict the lifetime of the pull-down device in the GOA circuit instead of the conventional one by $V_{TH}$ shift method. A new current-stress time degradation formula for the a-Si:H TFT is presented and verified well with experimental results. Concerning the effect of ON current of a-Si TFT was suitable to present the real TFT driving ability, it is also suitable for the analysis of TFT lifetime.

## 6. Acknowledgements

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## 7. References

[1] C. S. Chiang, J. Kanicki, and K. Takechi, Jpn. J. Appl. Phys., p. 4704 (1998)

[2] M. J. Powell, Appl. Phys. Lett. 43 p.597 (1983)

[3] F. R. Libsch and J. Kanicki, Appl. Phys. Lett., 62 (11), p. 1286 (1993)

[4] Hugues Lebrun, Nicolas Szydlo and Eric Bidal, The 22nd International Display Research Conference, IDRC'02, EURODISPLAY, p. 83 (2002)

[5] Chun-Ching Wei, Wei-Chung Lin, Shih-Hsun Lo, Chun-Jong Chang and Yang-En Wu, IDW'05, AMD11-3, p.1023(2005)