Advanced Packaging Technologies in Japan

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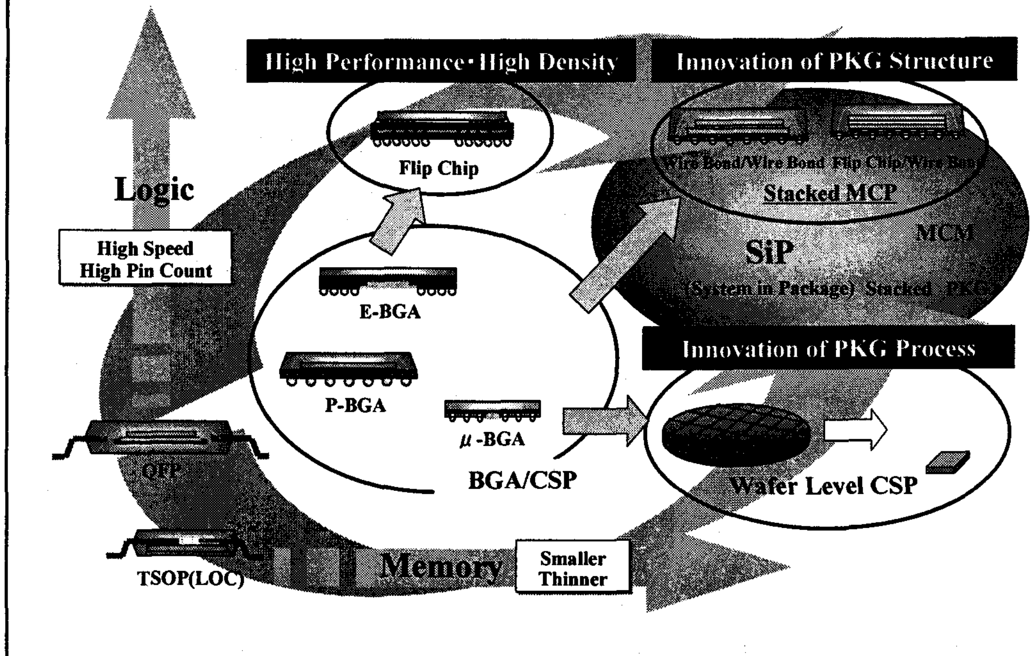
Contents

1. System Package Technologies in Japan
2. Through Si Technologies
3. Thin Si Wafer Technologies
4. New Wiring using Ink- jet Printing

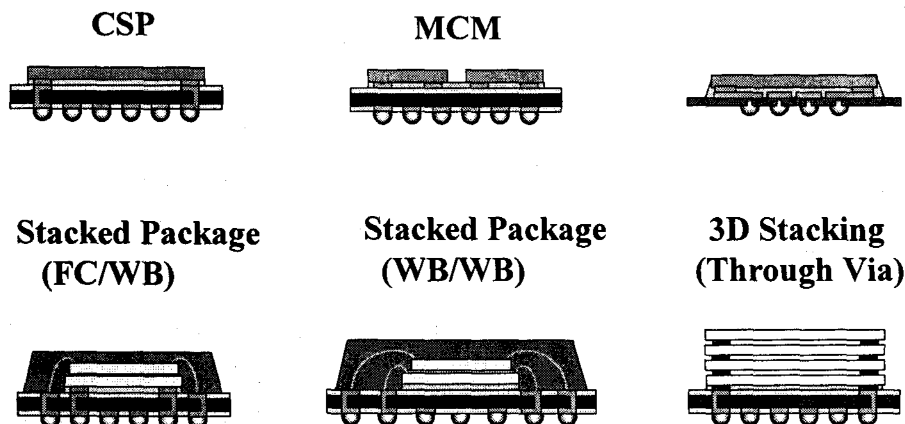
Trend of Semiconductor Packages



Increasing Packaging Consortium in Japan

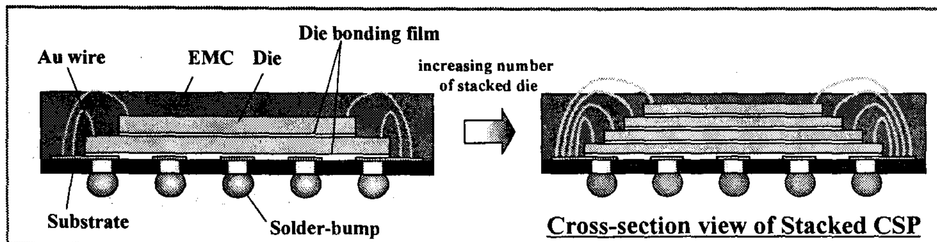
- SIP Consortium
- EWLP (Embedded Wafer Level Packaging) Consortium
- Yokohama High Density Packaging Consortium
- Micro-joining Research Committee

Example of Various SiP Technologies

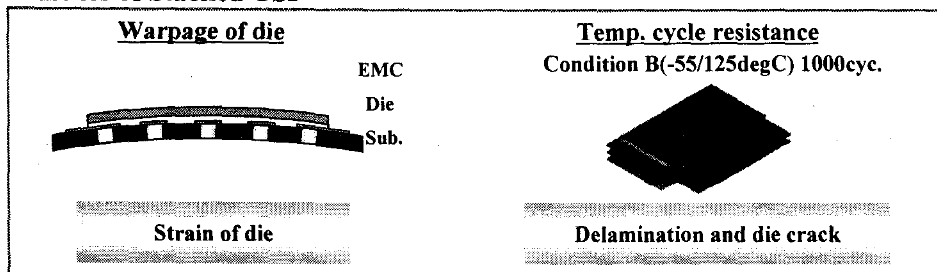


Packaging Materials for SiP

➢ Structure of Stacked CSP

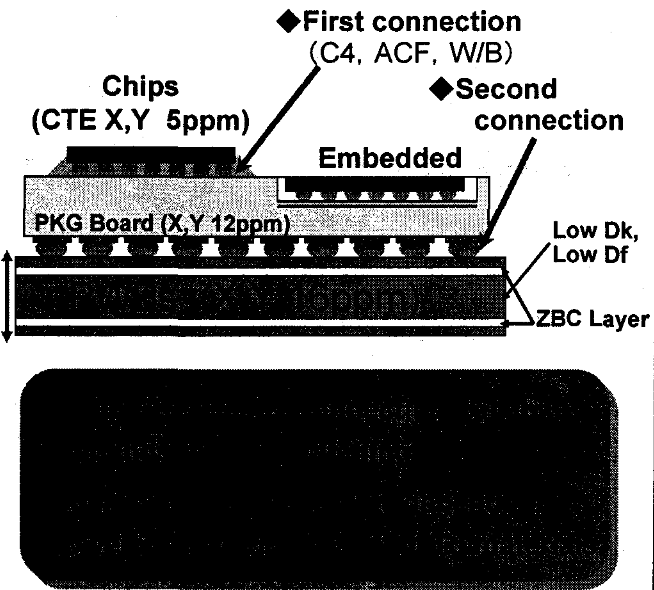


➢ Issues of Stacked CSP



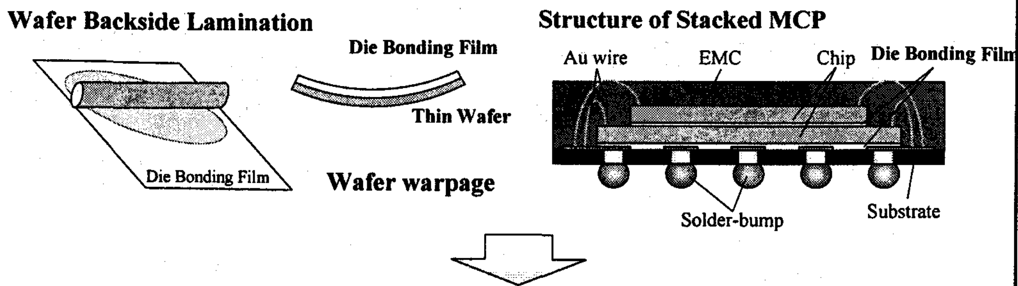
Technical key points of PWB Materials

- CTE Matching
- Micro-via
- Embedded
- Low Warpage
- Finer Line / Space (High Peel strength)
- Dimensional Stability
- High Speed
- High Frequency
- Environmentally Friendly (Lead-free,Halogen-free)
- High heat Resistance
- Low Water Absorption
- High Tg
- Through Hole Reliability
- Low CTE Z
- CAF Resistance

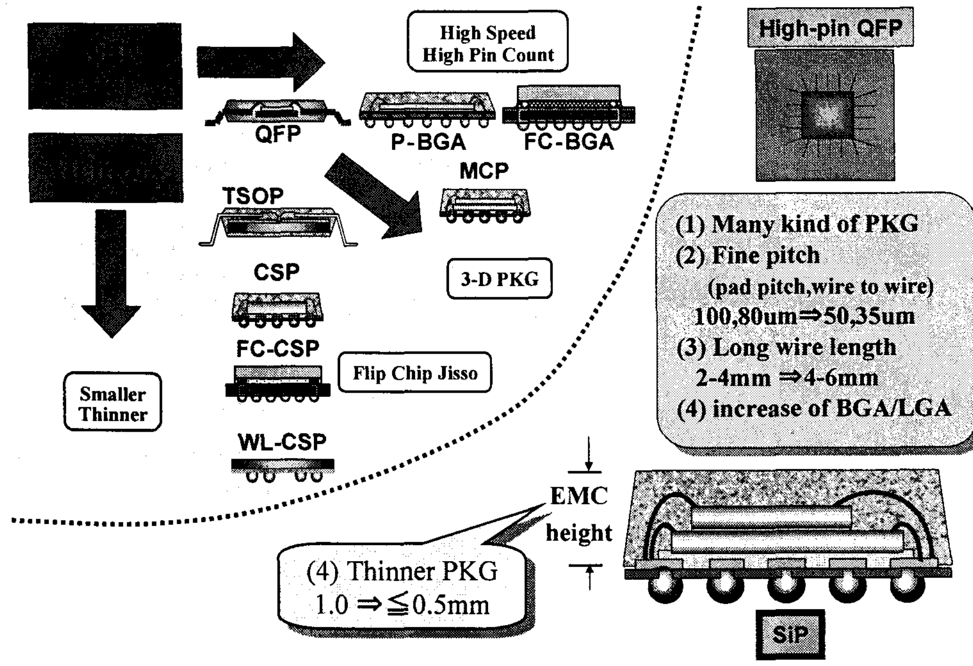


CTE : Coefficient of Thermal Expansion

Requirement for Die Bonding Film



- Reflow crack resistance : Higher adhesion
- Warpage deformation & thermal cycling resistance :
  Optimization of material properties(Modulus, C.T.E.)



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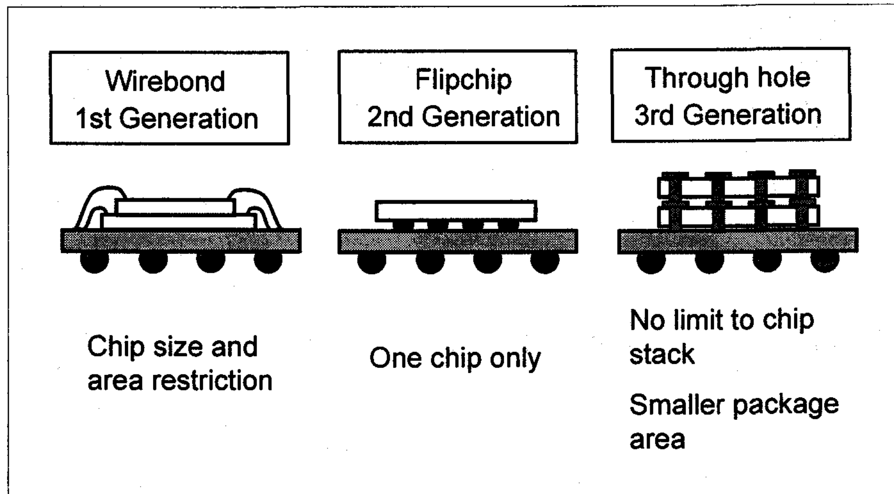
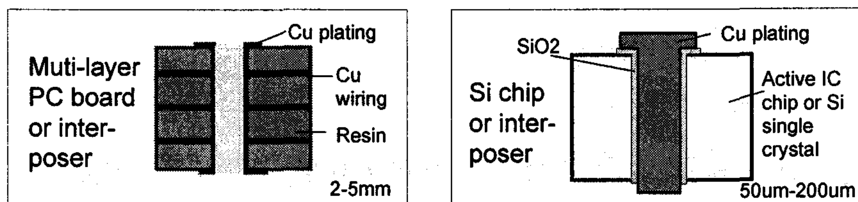
Chip connection



Silicon through hole

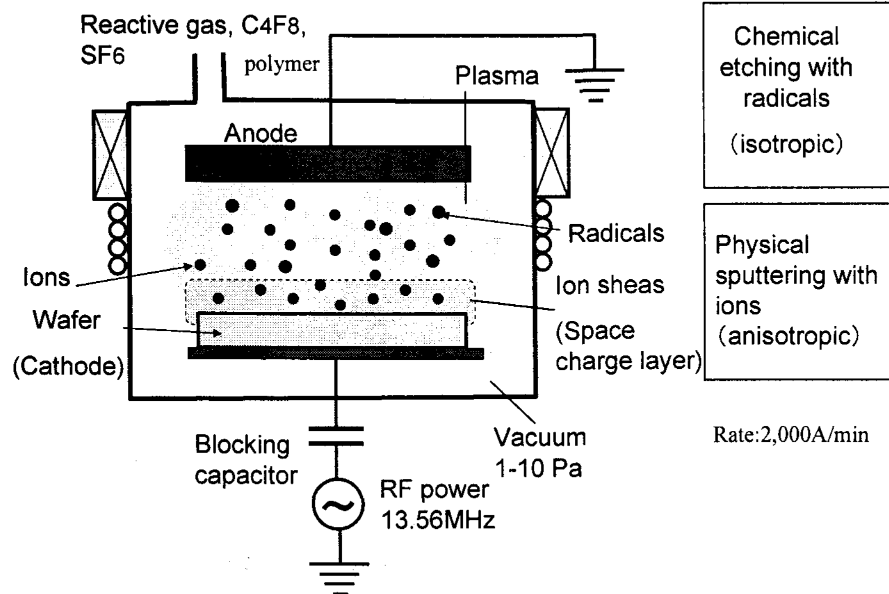


- Stands higher temperature, 400 degrees C
- Low thermal expansion - Si, 4ppm
- High insulation of SiO_2 - few MΩ
- Accurate dimension - 5um
- Small diameter - 20um
- Thickness - 50um
- Good HF characteristics
- MEMS technology

Major applications

- Through vias for active chips
  - Low resistivity silicon
  - Process temp. below 250 degrees C
  - High density finer holes
- Package interposer
  - Arbitrary silicon resistivity
  - Stands high temp. 400-600 degrees C
  - Larger process freedom

Reactive ion etching (RIE) (Deep etching)

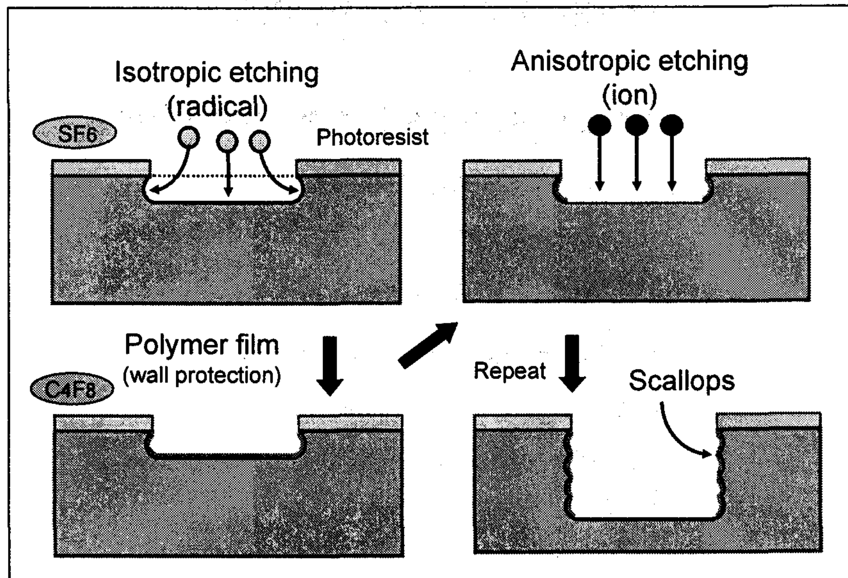


Chemical etching with radicals (isotropic)

Physical sputtering with ions (anisotropic)

Rate:2,000A/min

Bosch process RIE deep etching



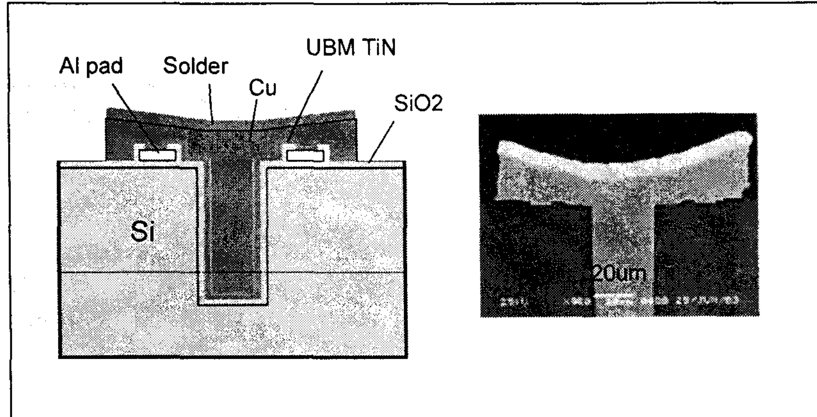
Dr.Franz Laemer,Bosch GmbH

High rate deep RIE development

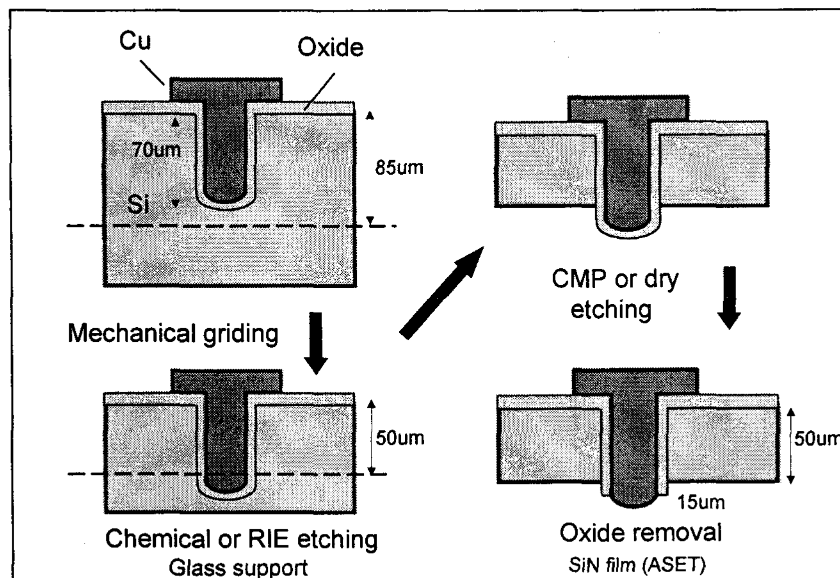
Basic pararell plate RIE, 0.2um/m
Bosch Process, 3um/m
NLD, Ulvac, 20um/m
ICP RIE, Sumitomo-STS, Bosch2, 25um/m
ICP Canon-Alcatel
ICP Samco, Bosch2
ICP DSE, Unaxis, Bosch2, 20um/m
Magnetron RIE, Epson, 45um/min

ICP:Inductively coupled plasma
NLD: magnetic neutral loop discharge

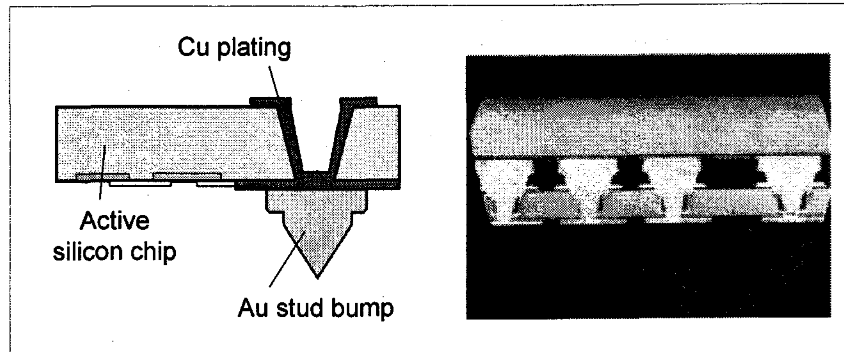
Cu Plating on the Through hole



Backside bump formation



Gold bump squeeze-in at RT
Hitachi-Renesas



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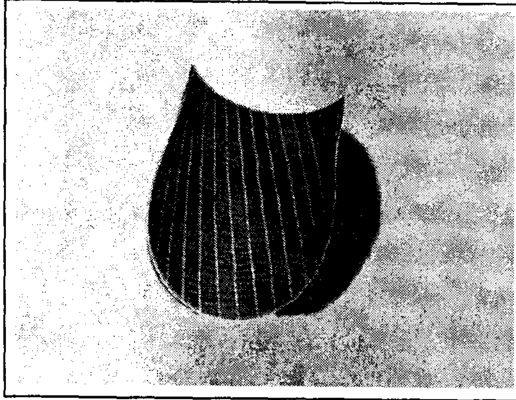
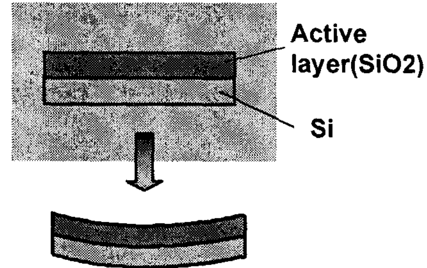
Warpage of Thin Si Wafer (Bimetallic Effect)



50um thickness of Si Wafer
(by Shinko Electric Industries)

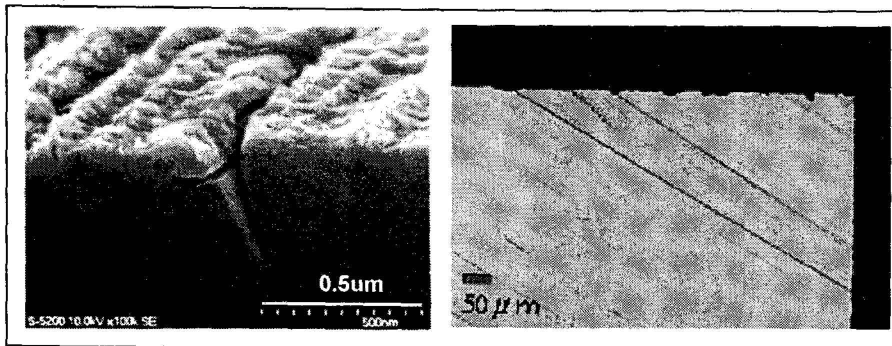
High Temp. ⇨ Room Temp.



Si wafer bends more as the thickness of Si wafer decreases.

CTE (Si):4ppm
(SiO2):0.5-12ppm

Edge Chipping during Dicing



Elimination of Warpage Issue of Thin Wafer

Courtesy of Disco

Thicken the edge of thin Si wafer

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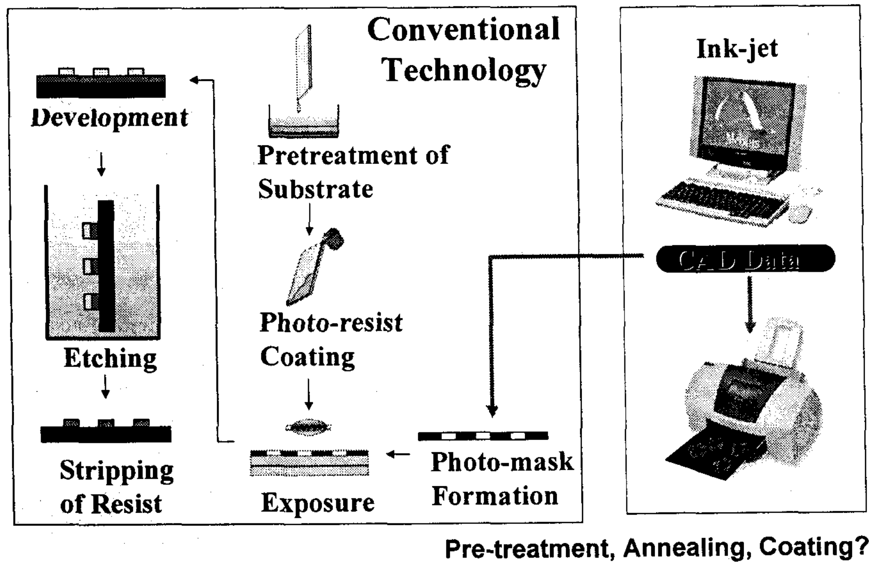
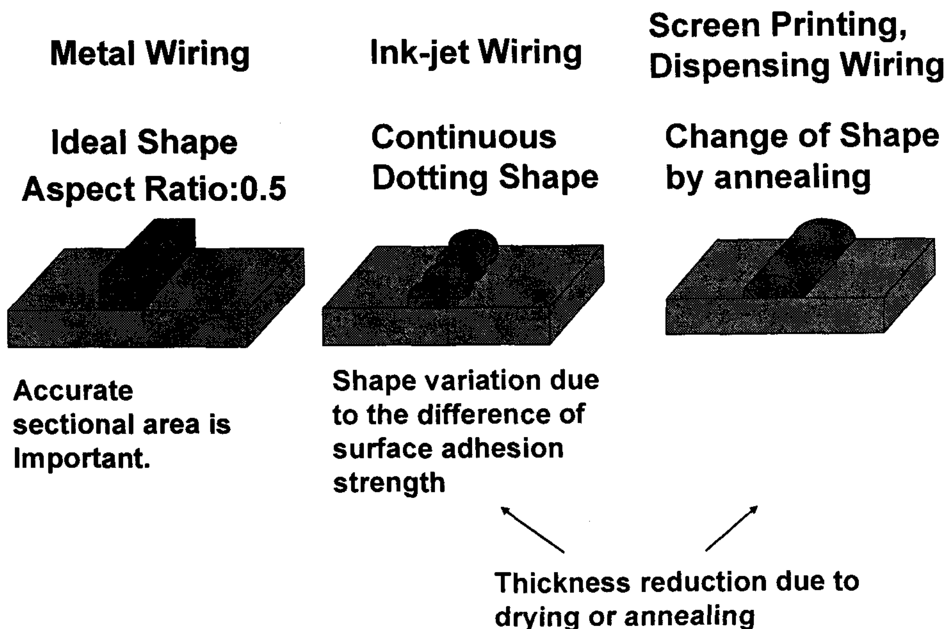
Mask free Metallizing by Ink-jet Printing Technology



Pre-treatment, Annealing, Coating?

Sectional Shape of Circuit



Thickness of Metal Wiring using Ink-jet Printing Technology

Drawing by nano-particles Ink-jet

Droplet:2pl, 15um diameter

50um diameter

Thickness reduction (20-80%) due to particle density

Annealing:150-300 degrees C

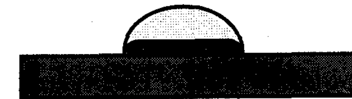
t:1-2um

Thick wiring by multiple coating

t:4-8um

Essential Study Items

- Nano-Metal (Ag,Au) Diameter:5nm,15nm
- Concentration of nano-particles:30-62%
- Ink Viscosity:5-20mPa.s
- Improvement of IJ equipment :Piezo electric
- Dot diameter:depends on surface treatment of substrate and ink viscosity 100um⇒60um⇒15um



Diameter:15um, Thickness:1-2um