3D Packaging:
Where All Technologies Come Together

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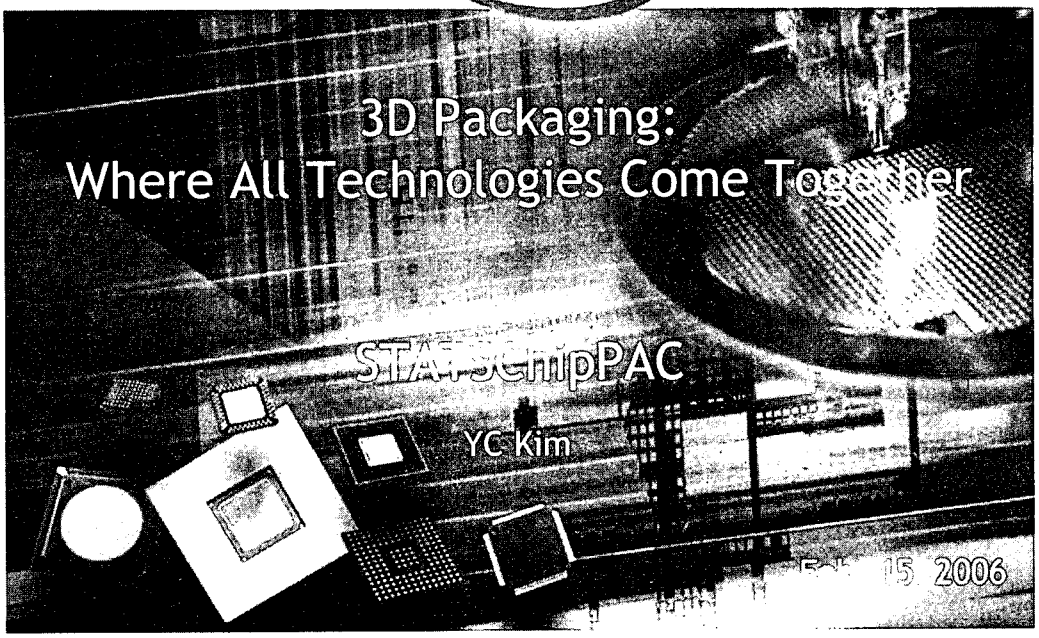


3-D Packaging

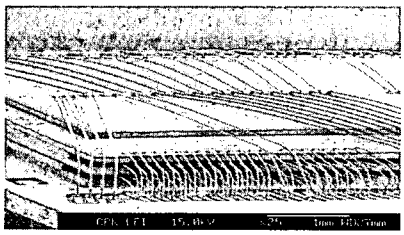
Contents

- ▷ Why 3-D?
- ▷ 3-D packages example
- ▷ Technology synergies and trade-offs
- ▷ Conclusions

3-D Packaging

Why 3D?

- Functional integration in a Small & thin package
- Lower cost
- Design flexibility
- Established supply chain
- Short time-to-market
- Higher reliability
- RoHS compatible
- Compelling advantages and low risk



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3-D Packaging

Challenges of 3-D Packaging

"More die in a thinner package"
"Final test"

- A thinner package needs thinner layers, stretches the performance envelope of all assembly processes, materials and equipment
- Final test cost and complexity drives design for test and migration to stacked-packages instead of stacked-die

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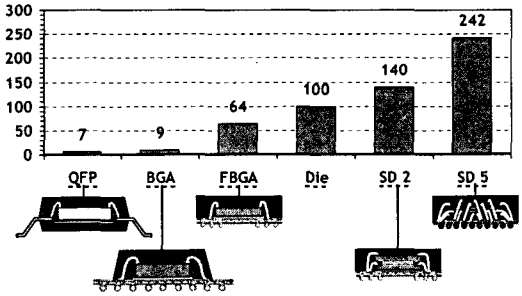
Functional Integration in Small Thin Package

Wireless application:
ASIC+ 2xFlash + SDRAM +
2x Spacers(6 chips)

Silicon / Package:
Area ratio increasing



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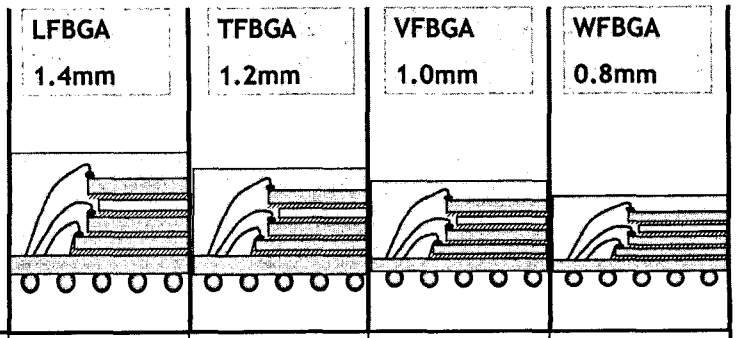
3-D Packaging

Stacked-Die CSP Roadmap

xFBGA type
Max. height



Dimensions are mm	LFBGA	TFBGA	VFBGA	WFBGA
Mold cap thickness	0.80	0.65	0.55	0.45
Die thickness	0.115	0.100	0.075	0.050
Substrate thickness	0.21	0.21	0.16	0.13
Ball dia.	0.40	0.35	0.30	0.25
Total	1.40	1.20	1.00	0.80

More chips in a thinner package

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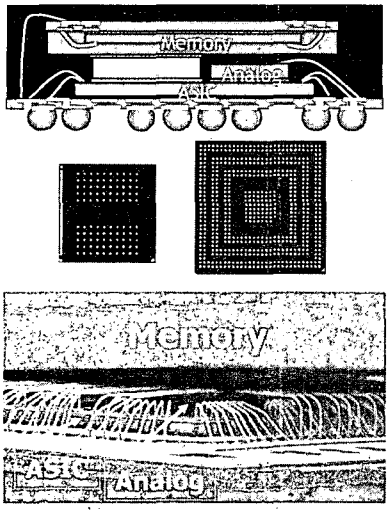
Package-in-Package (PiP)



- A mixed stack of die+package
- Stacked memory in top LGA(ISM)
- Stacked ASIC + Analog + other in bottom BGA
- Standard assembly process & materials, just like stacked-die CSP
- Thinner package, design flexibility
- Pre-tested LGA and simplify PiP test and maximize yield

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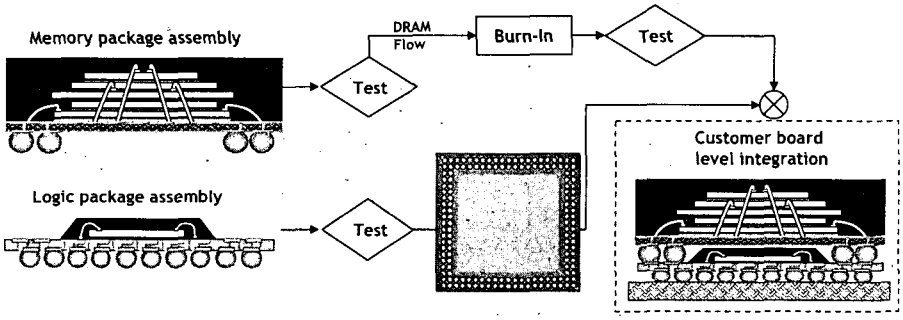
Package-on-Package (POP)

Baseband + Memory (NOR, NAND, DDR)



- PoP final assembly and test by OEM
- z-interconnect with solder ball increases body size, limits die stacking in bottom BGA

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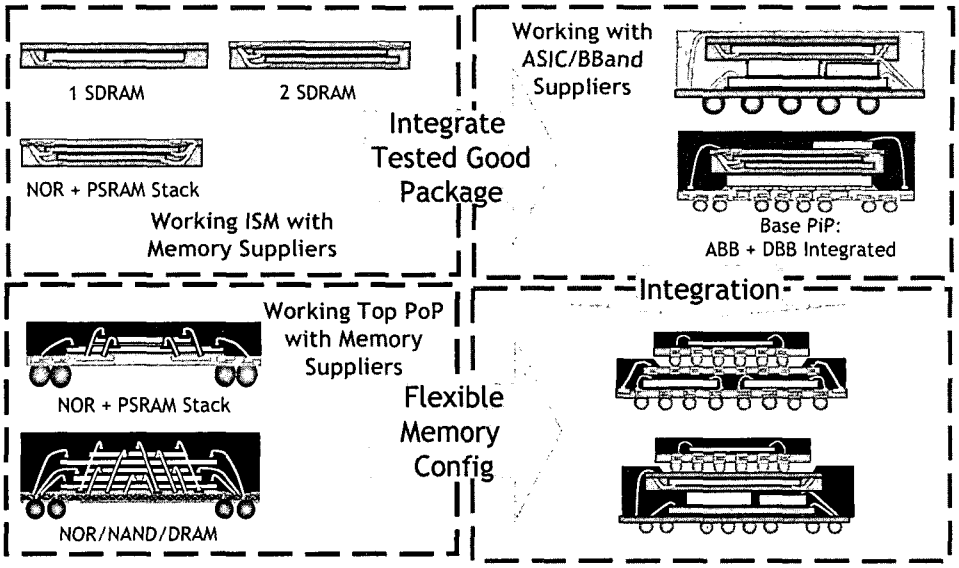
PiPPoP (Fan-in PoP)



- Future integration PiP and PoP type for memory configuration flexibility

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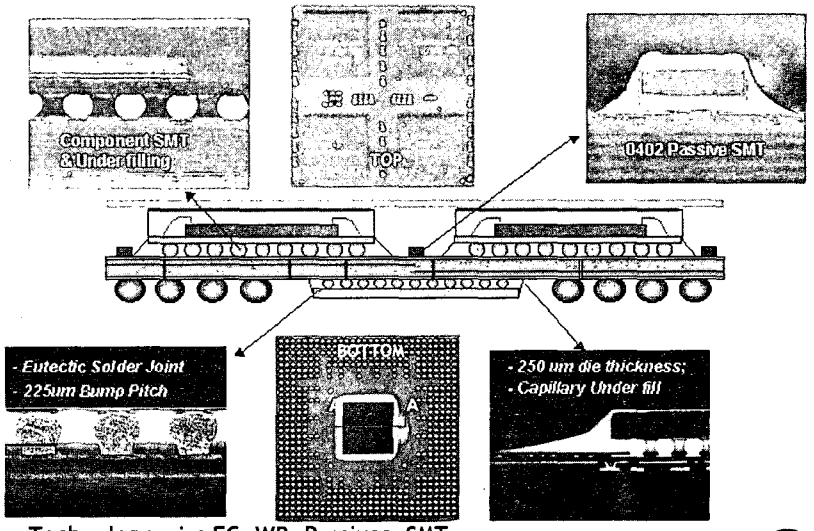
Computer Graphics Module

GPU+4xDDR+32xPassives+H/S



- Technology mix: FC, WB, Passives, SMT

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Technology Synergies & Trade-offs

- Wafer thinning, sawing
- Die attach materials, spacer technology
- Low loop wire bond, overhang, multi-row, Fine bond finger pitch
- Thin mold, Top Center Mold Gate
- Low-k, Circuit Under Pad (CUP)
- Thin, dense substrates, fine pitch ball attach
- Module design, modeling, performance testing

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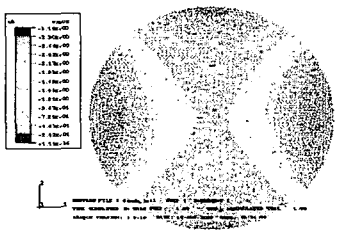
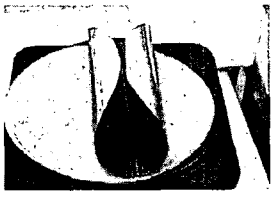
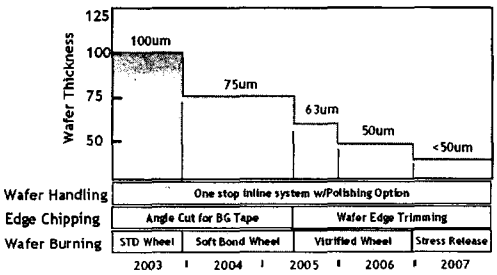
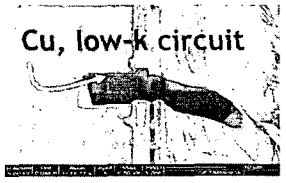
Wafer Thinning & Dicing saw









- In-line back grind, polish, D/A film, saw tape lamination
- Wafer saw two-step cut or laser, attention to metal peel, low-k damage

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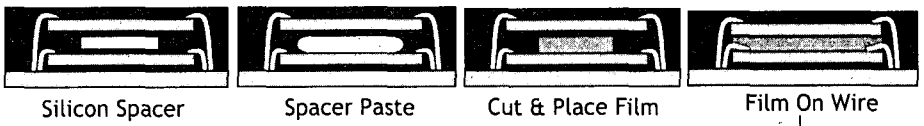
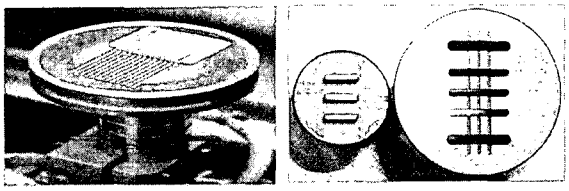
Die Attach Technology

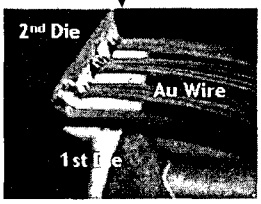
- Thin bond line ,film adhesive or epoxy paste (conductive or non-conductive)
- Multi-layer structure, stress, voids, cost
- Spacer: silicon, epoxy, film



Silicon Spacer | Spacer Paste | Cut & Place Film | Film On Wire



Thin die kit (Needleless type)



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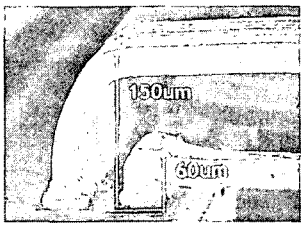
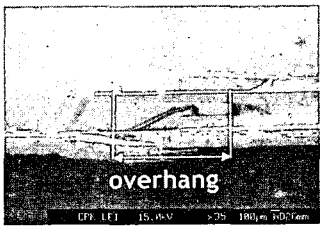
Enabling technologies for 3-D Packaging

Wirebond on Overhang, Low loop, Multi-row





Loop height	
FRW	60um
RVRS	50um

Die Thick (um)	Overhang (mm)
100	2.0
75	1.5
50	0.7

Wirebond pitch	
1-row	40um
2-row	25/50um
3-row	20/60um

- Bond loop height and shape control critical.

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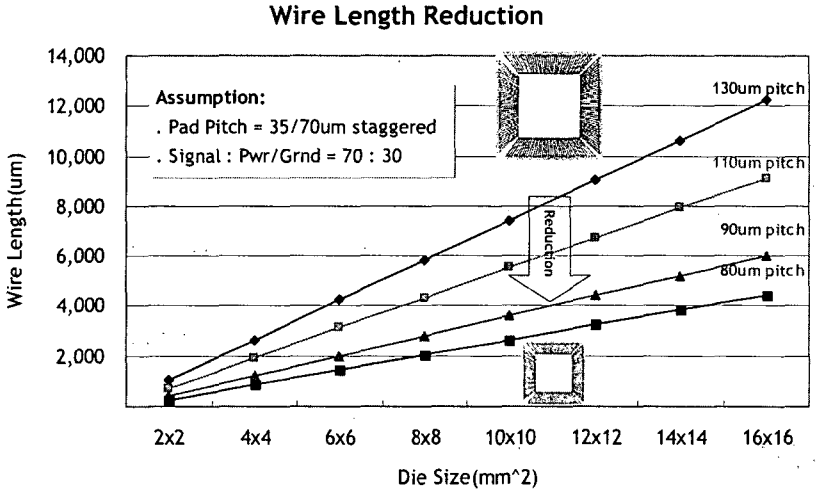
Fine Bond Finger pitch



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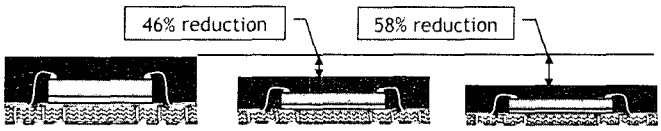
Enabling technologies for 3-D Packaging

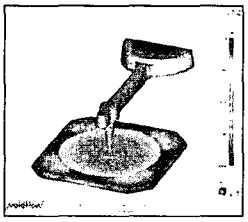
Thin core substrate & Mold Cap



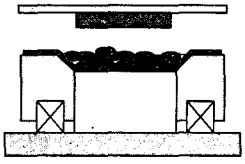
- > 250um Gap
- 0.45mmT Mold
- 0.26mm T PCB
- 100um core

- <150um Gap
- 0.25mmT Mold
- 0.13mm T PCB
- 60um core

- <100um Gap
- 0.20mmT Mold
- 0.10 mm T PCB
- 40um core



Top Center Mold Gate



Free Flow Thin mold

- Thin core Substrate
- Thin mold cap for stacked-die and stacked-package
- New mold technology like TCMG, Vacuum, FFT

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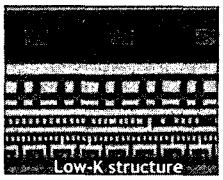
Enabling technologies for 3-D Packaging

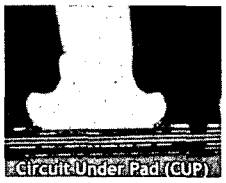
Low-k dielectric, CUP

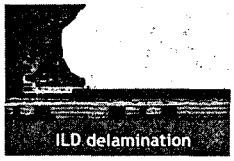
- 90nm, 65nm Low K as k < 3.0
- 45nm/Ultra Low K as k < 2.6
- CUP(circuit under pad) is trend in bond pad layout

- *Major dielectric materials are ;*
  Non-polymer type is black diamond & Coral.
  Polymer type is SiLK.

- **Challenges for Assembly**
  Chipping & Chip Interlayer delamination @ Sawing
  Pad peeling & collapse @ wire bonding
  Electrical function shift due to PKG stress
  ILD delamination in thermal cycle stress







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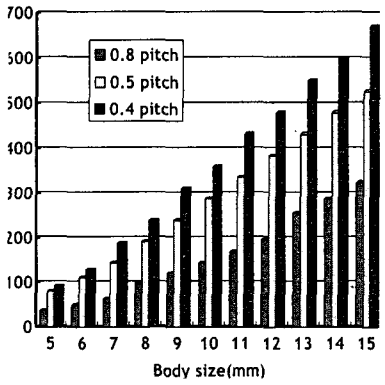
Fine solder ball pitch



Body size	Ball count / Ball pitch		
	0.80	0.50	0.40
15x15	324	528	672
14x14	289	480	600
13x13	256	432	552
12x12	196	384	480
11x11	169	336	432
10x10	144	288	360
9x9	121	240	312
8x8	100	192	240
7x7	64	144	188
6x6	49	112	128
5x5	36	81	92

- Fine pattern substrate with 30/30 Trace pitch, VIP/VOP, Tailless, Pad finish (CuOSP)
- SBM capability for small solder ball and pitch

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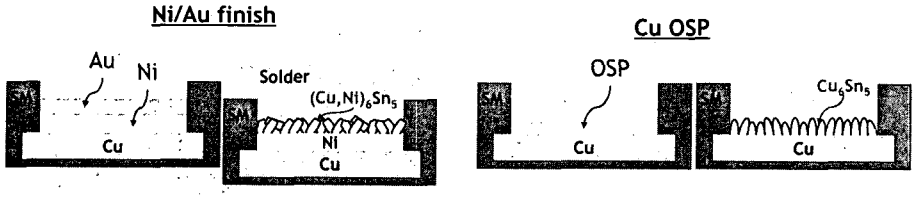
Solder joint

For Hand held product, BLR is important, especially Drop shock test.
RoHS, Pb free Solder ball requirement



Solder Alloy SAC405 or SAC305 → For Mobile Devices → Ni doped Low Ag (Sn1.2Ag0.5Cu+Ni)

Ball Pad Finish Ni/Au → Cu OSP

The combination of Ag & Cu acts as below
- Lower melting point
- Increase strength
- Improve fatigue property

Low Ag acts as a shock buffer
Ni dopant acts as below ;
- increase strength
- inhibit the growth of brittle IMC (Secondary IMC, Cu_3Sn)

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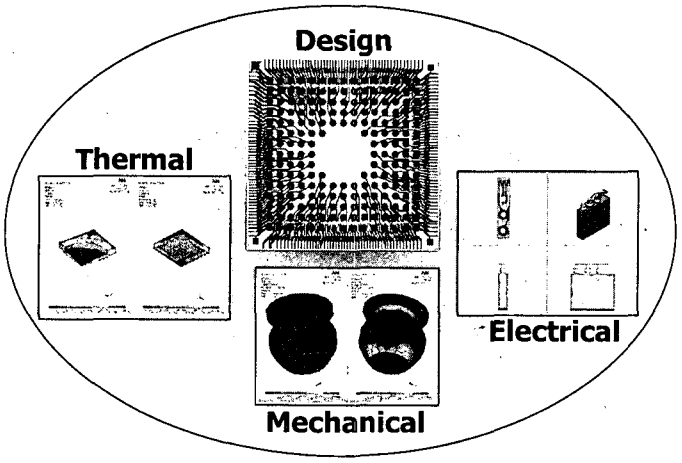
Enabling technologies for 3-D Packaging

Design, Modeling/Simulation Performance Test



- Together insure success at first pass

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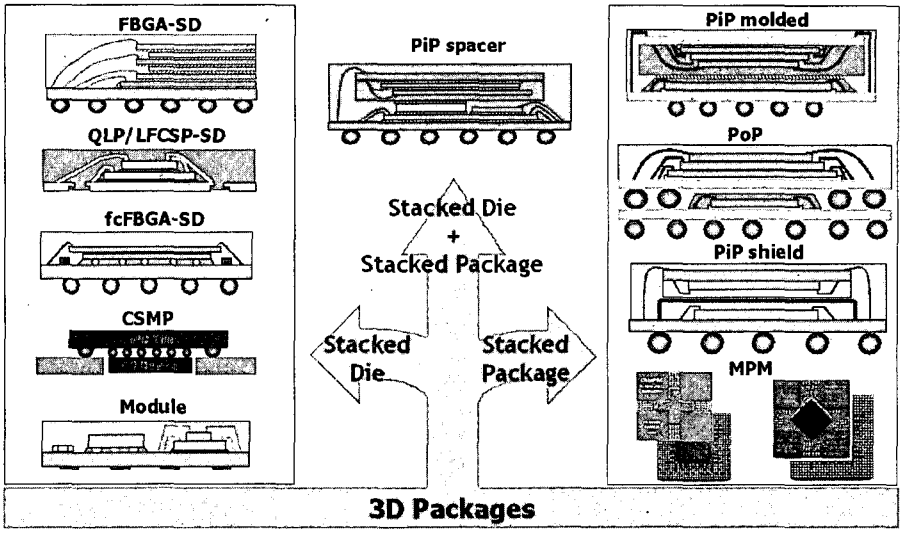
3D-Package Directions



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Summary

- 3D is proliferating in all package types
- Thin packages challenge all assembly technologies
- Package assembly and test are closely coupled and design for testability is imperative to success

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