A-7

Effects of Surfactant Molecular weight and Concentration in Nano-Ceria Slurry on Nanotopography Impact in Chemical Mechanical Polishing

Hyuk-Yul CHOI, Hyun-Goo KANG, Jun-Seok KIM, Ungyu PAIK*, Jea-Gun PARK†

Nano-SOI Process Lab. Hanyang University; *Department of Ceramic Engineering, Hanynag University
(parkjgl@hanyang.ac.kr†)

Chemical mechanical polishing (CMP) iswidely used to planarize the wafer surface during the device manufacturing. Recently, the "nanotopography" of the silicon wafer has become an important issue in Shallow Trench Isolation (STI)-CMP process, since it seriously affects the post-CMP film thickness variation. We investigated the dependency of nanotopography impact on surfactant concentration and Molecular weight in ceria(CeO_2)slurry as one of the key factors in STI-CMP process.

The slurries were prepared with different organic surfactant concentration from 0to 0.8 wt% with different molecular weight of 5K, 30K, and 90K. The plasma-enhanced tetra-ethyl-ortho-silicate (PETEOS) films were polished with a Strasbaugh 6EC. The nanotopography variation was measured by Nano-Mapper (ADE).The oxide film thickness variation of the wafer before and after CMP was measured with a reflector meter NanoSpec 8300 (Nanometrics).

The profiles of the oxide (SiO_2) thickness deviation (OTD) after CMP coincided well with those of the nanotopography variation, which means the OTD after CMPwas mainly caused by the nanotopography. We controlled the polishing time tokeep a constant removal depth of 3000 Åthrough the slurries including various concentrations of the surfactant and molecular weight in ceria slurry. The standard deviation of OTD amplitude was calculated and we found the results as follows: 1) The OTD after CMP increased according to the increase of the surfactant concentration. 2) This trend (1) was more remarkable for higher molecular weight of surfactant in slurry suspension. The mechanisms onthese result is discussed and attributed to the surfactant adsorption on thefilm surface.

The Korea Ministry of Science and Technology supported this work through the National Research Laboratory (NRL) program. We thank SUMCO Corp. and Hynix Semiconductor Inc. for helping us with our experiments.

Keywords: Nanotopography, STI-CMP, Ceria, Molecular Weight

A-8

Origin of Void Formation in a Porous Anodic Alumina Template on Si wafer

Hong-Seok Seo, Yang-Gyoo Jung, Sang-Won Jee, Han-Don Um, Jung-Ho Lee†

Dept. of Fine Chemical Engineering, Hanyang University
(jungho@hanayng.ac.kr†)

Preparation of a porous anodic alumina (PAA) template, directly formed on Si wafer, enables high density, size-controlled nanowire arrays which are then vertically integrated over wafer-scale areas to fabricate nanodevices, such as field-effect-transistors and sensors. The presence of interfacial voids between the alumina film and Si substrate, however, complicates the organization of reliable contacts between the nanopores (or nanowires) and substrate (or bottom electrodes). We describe a complete process of void formation according to the inversion behavior of the barrier layers. We also clarified that the alumina transformation of the Almetal remaining when the barrier layer of nanopores touched the substrate purposely nucleated the interfacial voids so as to accommodate the stresses of volume expansion without devastating the pore arrays.

Keywords: Porous anodic alumina, Void, Volume expansion, Additional space, Inverted barrier layer, Si wafer