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Effects of Amorphous-silicon and Poly-silicon films on Within-Wafer Non-Uniformity (WIWNU) Improvement in Chemical Mechanical Polishing.

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As device dimensions continue to decrease and the leading-edge feature size becomes smaller than 0.7 um, the chemical mechanical polishing (CMP) process must be capable of removing a very thin layer of poly-silicon and oxide films with flat surface to form the floating gate in NAND-flash memory application. In addition, CMP technique has been considered to improve the surface uniformity of the poly-silicon film to increase its carrier mobility. The dielectric films whether deposited or thermally grown on such polished poly-silicon present excellent breakdown properties and much lower junction leakage. However, in contrast to its popular applications of CMP, the mechanisms to improve the surface uniformity of poly-silicon films, especially for the poly-silicon involved in the chemical reaction between slurry and film surface during CMP process, are unknown in detail. In this study, therefore, we investigated the effects of the amorphous-silicon and poly-silicon films on surface uniformity improvement by performing CMP process. The amorphous-silicon film was deposited on the oxidized substrate in an LPCVD system at 530 °C. The poly-silicon film was deposited by rapid thermal annealing (RTA) treatment for 15sec at 930 °C after amorphous-silicon film formation. The films were polished with a Strasbaugh 6DS-SP. The films thickness variation of the blanket wafer before and after CMP was measured with Nano-spec 180 (Nanometrics) and Ellipsometer (Ellipso technology). The depth of line profile in remaining films was measured by SEM (Hitachi) and AFM (PSIA). We found that not only improved the film surface uniformity and optimized process condition during CMP process. For the amorphous-silicon film, film surface uniformity after CMP is better than the poly-silicon film at a same experimental condition will result in higher surface planarity for commercial slurry. In optimized CMP process condition, the rotation speeds of both the head and the table were 30 (low) rpm, and the directly head pressure was 3 (low) psi. The slurry flow rate was 100 cm^3/min and the polishing time was 30 s.

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Keywords: WIWNU, CMP, slurry, Poly-silicon films, Amorphous silicon films

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Reduction of Large Particles and Light Point Defects (LPD) by Aging and Selective Sedimentation Process in Ceria Slurry for Shallow Trench Isolation Chemical Mechanical Polishing

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In contemporary ULSI fabrication, chemical mechanical polishing (CMP) is an essential process, and shallow trench isolation (STI) process is one of the most important applications of CMP technology. Recently, it is the ceria slurry that enables the application of STI-CMP, in which the selectivity of removal rate between oxide (SiO_2) and nitride (Si_3N_4) layers is a critical factor. Ceria slurry with an organic additives shows higher oxide-to-nitride selectivity than fumed silica based slurry. However, the ceria slurry has a major disadvantage which is defects on the film surface, which can be induced with only a small amount of large particles. In this study, therefore, we investigated the aging and sedimentation process of ceria slurry on slurry characteristics, such as the particle size distribution, the large particle count and the dispersion stability and remaining light point defects (LPD) on wafer surface during the STI-CMP. In addition, we confirmed that the aging time and temperature were considered as important variables which give more influences on slurry characteristics in STI-CMP. By using aging and sedimentation process, large particles produced by either hard agglomeration or soft flocculation in ceria slurry were reduced and the dispersion stability of ceria particles in the slurry could be also improved. In the CMP evaluation, as a result, defects on wafer surface were significantly restrained, while maintaining the reasonable oxide removal rate and oxide and nitride selectivity.

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Keywords: aging, sedimentation process, large particles, ceria, STI-CMP, defect