A New High Frequency Linked Soft-Switching PWM DC-DC Converter with High and Low Side DC Rail Active Edge Resonant Snubbers for High Performance Arc Welder

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Abstract—This paper presents a new circuit topology of dc bus line switch-assisted half-bridge soft switching PWM inverter type dc-dc converter for arc welder. The proposed power converter is composed of typical voltage source half-bridge high frequency PWM inverter with a high frequency transformer link in addition to dc bus line side power semiconductor switching devices for PWM control scheme and capacitive lossless snubbers. All the active power switches in the half-bridge arm and dc bus lines can achieve ZCS turn-on and ZVS turn-off commutation operation and consequently the total turn-off switching losses can be significantly reduced. As a result, a high switching frequency of using IGBTs can be actually selected more than about 20 kHz. The effectiveness of this new converter topology is proved for low voltage and large current dc-dc power supplies such as arc welder from a practical point of view.

I. INTRODUCTION

A. Research Background

Recently, saturable inductor assisted ZVS-PWM full-bridge high-frequency inverter link dc-dc power converter [1] and lossless capacitors and transformer parasitic inductive components assisted soft switching dc-dc power converter with phase-shifted modulation control scheme in secondary-side of high frequency transformer [2]-[3] have been developed and evaluated. These power converter circuit topologies are suitable for handling high output power more than about several kW, especially for high voltage and low current applications as new energy related power supplies. However, secondary magnetic switches or transformer secondary side semiconductor switching devices in these converter circuit topologies may cause large conduction loss when these power circuit topologies are adopted for low voltage and large current application as arc welding power supplies. Therefore, for the low voltage and large current application required for arc welding power supplies, a soft switching dc-dc power converter with active switches in the primary side of high frequency transformer is considered to be more suitable and acceptable.

B. Research Objectives

This paper presents a novel circuit topology of voltage source half-bridge type soft switching PWM inverter. Under the newly-proposed high frequency inverter link dc-dc power circuit, all the active switches in the half-bridge arm and dc bus lines can actively achieve ZCS turn-on and ZVS turn-off commutation operation.

The steady state operating principle of the proposed soft switching PWM dc-dc power converter is described with its remarkable features. The experimental operation results of this new type of soft switching PWM dc-dc power converter using IGBT power modules are illustrated including power loss analysis as compared with that of the hard switching PWM dc-dc power converter. The practical effectiveness of the proposed high frequency transformer link dc-dc power converter acceptable and suitable for high power applications which is designed for low voltage and large current output is actually proved on the basis of experimental data.

II. NEW SOFT SWITCHING DC-DC CONVERTER

Fig. 1 shows the proposed soft switching PWM dc-dc converter circuit using a novel type half-bridge soft switching PWM inverter with high frequency transformer link. Proposed converter is composed of typical voltage source half-bridge inverter with a active PWM switch $Q_3(S_3/D_3)$ in positive dc bus line and a active PWM switch $Q_4(S_3/D_3)$ in negative dc bus line and two lossless snubbing capacitors C_1, C_2 and two diodes D_5, D_6. Two centre points of two capacitors C_1, C_2 and two diodes D_5, D_6 are connected to a mid point of two voltage sources E_1, E_2 and one of terminals of primary winding of high frequency transformer. The voltage of two voltage sources E_1, E_2 and capacitance of capacitors C_1, C_2 are designed so as to be equal ($E_1=E_2=E$, $C_1=C_2=C$). The main active switches $Q_1(S_1/D_1)$ or $Q_2(S_2/D_2)$ can be turned on and turned off in accordance with modified PWM control circuit similar to conventional half-bridge type hard switching PWM inverter.

The switches in the half-bridge type inverter can perform ZVS turn-off transition due to the presence of the active PWM switches Q_3 or Q_4 which are turned off and the snubbing capacitors C_1 or C_2 are completely discharged before the active switches Q_1 or Q_2 in half-bridge type inverter arms are turned off. In addition, the inverter switches can also perform ZCS at a turn-on transition with the aid of inductance L_S, as a parasitic leakage inductance of high frequency transformer HF-T.

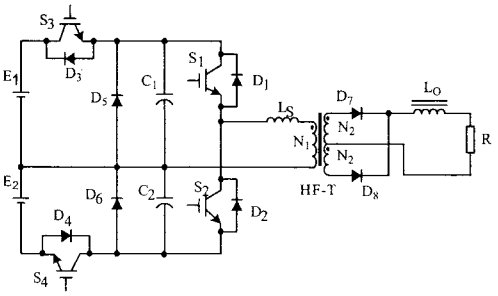


Fig. 1 Soft-switching PWM dc-dc converter using half-bridge PWM inverter with high frequency link.

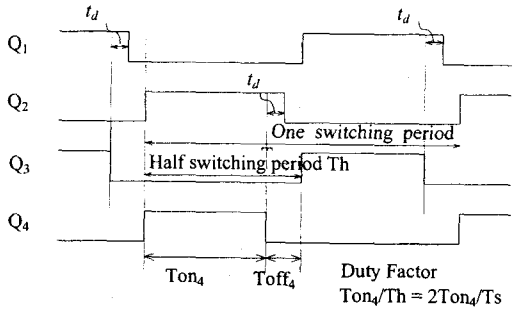


Fig. 2 Pattern sequences of switching gate driving pulses.

III. PRINCIPLE OF OPERATION

A. Gate Voltage Pulse Timing Sequences

Fig. 2 shows timing pattern sequences of switching gate driving pulses. The gate voltage pulse signals for the inverter switches Q_1 or Q_2 in voltage source half-bridge inverter arms are the same as PWM signal sequences of conventional half-bridge inverter. Regarding the turn-on gate voltage pulse signals to the dc bus line side series switches Q_3 or Q_4, the signals are applied to Q_3 or Q_4 at the same timing as the turn-on signals to Q_1 or Q_2, respectively.As for the turn-off signals to Q_3 or Q_4, the signals are delivered to Q_3 or Q_4 before the predetermined length of time t_d on the basis of the time when the turn-off signals are applied to Q_1 or Q_2. In other words, the turn-off pulse signals are applied to Q_1 or Q_2 after the turn-off gate signals are supplied to Q_3 or Q_4 by a time t_d.

B. Operation Modes

Fig. 3 illustrates the relevant operating waveforms in a complete switching period for the pulse pattern of gate drive timing sequences shown in Fig. 2. The operation modes are divided into seven operation modes from mode 0 to mode 6 in accordance with operational timing from t_0 to t_6 and each operation principle is described hereafter. The equivalent circuits corresponding to each mode are shown in Fig. 4.

1) Mode 0 : ~t_0 Before time t_0, the switches Q_1 and Q_3 are turned on. At this time, i_{tl} flows through the primary winding of transformer HF-T. Also, i_{s1} flows through Q_1 and i_{s3} flows through Q_3. In this period, all currents i_{tl}, i_{s1} and i_{s3} are equal and the voltage v_{C1} across the capacitor C_1 is the same as the dc bus line voltage E_1.

2) Mode 1 : t_0~t_1 At time t_0, the turn-off signal is applied to Q_3. At this time, the series switch Q_3 in dc bus line can be turned off with ZVS because the current i_{s3} through Q_3 is immediately cut off due to the lossless snubbing capacitor C_1. After time t_0, the voltage v_{C1} across the capacitor C_1 discharges constantly toward zero voltage from E1=E voltage. At this time, the voltage v_{C1} across the lossless snubber capacitor C_1 is estimated as,

$$v_{C1}(t) = E - (i_{tl}/C)t \qquad (1)$$

Where, i_{tl} is a primary current of high frequency transformer. From the eq. (1), the discharging time of the capacitor C_1 until v_{C1} becomes zero is given by,

$$t = CE/i_{tl} \qquad (2)$$

From eq. (2), the more the current i_{tl} though primary winding of transformer HF-T is large, the more the discharging time for capacitor C_1 is short. On the other hand, the more the current i_{tl} is small, the more the discharging time is long. Under this newly-developed circuit, the delay time t_d indicated in Fig.2 is designed so as to be longer than the time calculated from the eq. (2) under the condition of the maximum i_{tl} and the maximum output current. In this case, switches Q_1 or Q_2 can achieve ZVS turn-off transition completely. If we need to enlarge the complete ZVS operation range at the turn-off commutation for the switches Q_1 or Q_2, the delay time t_d should be varied according to the value of current i_{tl}.

3) Mode 2 : t_1~t_2 At time t_1, the voltage v_{C1} becomes zero. In the interval from t_1 to t_2, the diodes D_5 is turned on and the current i_{tl} through transformer primary winding flows through the circulation loop; $L_S \rightarrow D_5 \rightarrow S_1 \rightarrow L_S$.

4) Mode 3 : t_2~t_3 At time t_2, the turn-off gate pulse signal (see Fig.2) is applied to Q_1. At this time, the switch Q_1 can be turned off with ZVS because the voltage v_{C2} was already zero during last half operation cycle and the diodes D_2 of Q_2 are immediately turned on. After that, the capacitor C_2 is charged up to the same voltage as dc bus line voltage E_2. At this mode, the condition that the capacitor C_2 is just charged up to the same voltage as dc bus line voltage E_2 is can be estimated by eq. (3).

$$(1/2)CE^2 = (1/2)\,L_S\,(i_{tl})^2 \qquad (3)$$

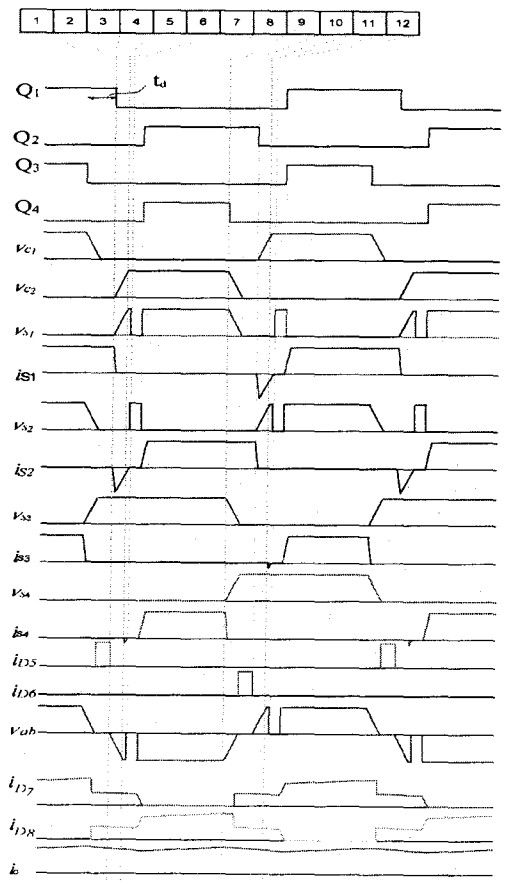
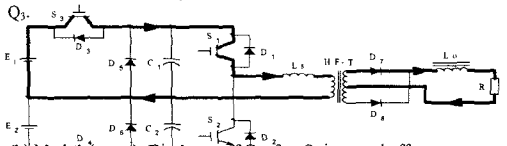
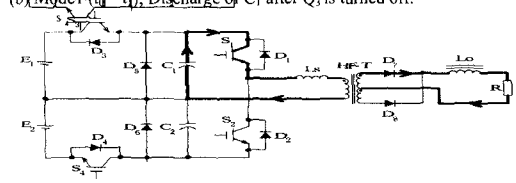


Fig. 3 Operating waveforms during one switching period.

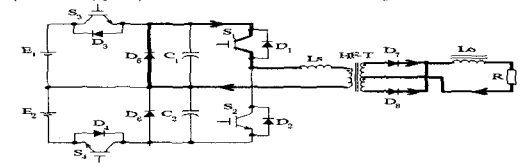
(a)Mode0 ($\sim t_0$); Energy transfer to secondary during turn-on of Q_1 and Q_3.



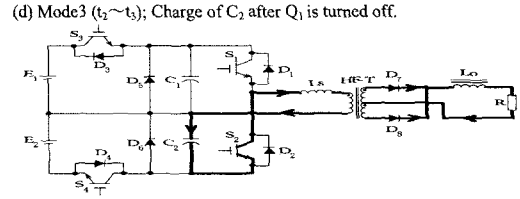
(b) Mode1 ($t_0 \sim t_1$); Discharge of C_1 after Q_3 is turned off.



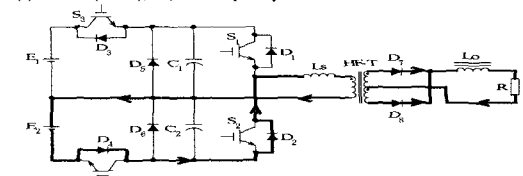
(c) Mode2 ($t_1 \sim t_2$); Current circulation after discharge of C_1.



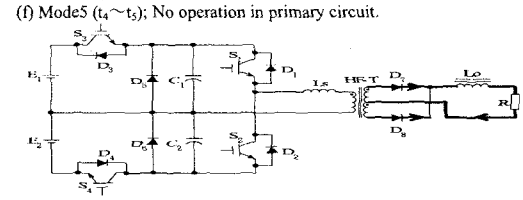
(d) Mode3 ($t_2 \sim t_3$); Charge of C_2 after Q_1 is turned off.



(e) Mode4 ($t_3 \sim t_4$); v_{C2} is clamped by E_2.



(f) Mode5 ($t_4 \sim t_5$); No operation in primary circuit.



(g) Mode6 ($t_5 \sim t_6$); Energy transfer to secondary during turn-on of Q_2 and Q_4.

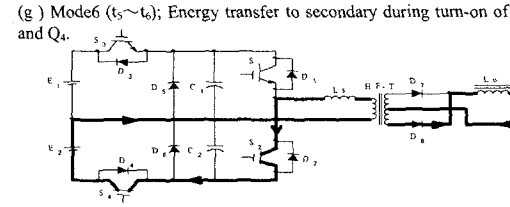


Fig. 4 Equivalent circuits for seven operational modes.

However, as described after in mode 6, circuit parameters should be designed to meet the condition of $(1/2)CE^2 \leq (1/2)L_S(i_{l1})^2$ in order to achieve ZVS commutation at turn-on transition of Q_4.

5) Mode 4 : $t_3 \sim t_4$

Under a condition of $(1/2)CE^2 < (1/2)L_1(i_{l1})^2$, after the voltage v_{C2} reaches the dc bus line voltage E_2, the voltage v_{C2} across the snubber capacitor C_2 is clamped to dc bus line voltage E_2 because the diode D_4 of Q_4 is turned on and the energy stored into leakage inductance L_S is back to dc bus line voltage source E_2.

6) Mode 5 : $t_4 \sim t_5$ In this mode, all operations are stopped in the primary circuit of transformer.

7) Mode 6 : $t_5 \sim t_6$ At time t_5, the turn-on gate pulse signals are applied to the switches Q_2 and Q_4. At this time, the switches Q_2 can be turned on with ZCS due to the parasitic inductance L_S of transformer HF-T. And more the series switch Q_4 in the bus line achieves ZVS/ZCS at turn-on transition because the voltage v_{C2} is the same voltage as dc power bus line voltage E_2. Thereafter, the operation processes for Q_2 and Q_4 are the same as that for Q_1 and Q_3 aforementioned and the operation processes for Q_1, Q_3 and Q_2, Q_4 will be repeated in sequence continuously.

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

A. Total System Implementations

The experimental setup circuit is shown in Fig. 5. In the setup implementation, the maximum output voltage and current are 36V,400A, respectively. The design specifications and circuit parameters are described in Table. 1. The whole appearance of experimental setup using arc welding power supply is presented in Fig. 6.

The maximum output of this experimental setup is 36V, 400A(14.4 kW). Connecting IGBTs and capacitor C_1, C_2, C_3 and C_4 by the printed circuit board enables to minimize the stray inductance at connections among IGBTs, C_1, C_2, C_3 and C_4. Actually, the minimum leakage inductance is particularly important on this new soft-switching PWM dc-dc converter, because spike voltage across collector and emitter of IGBTs easily appears at a turn off transition if there is wiring stray inductance between snubbing capacitors and the IGBT switches.

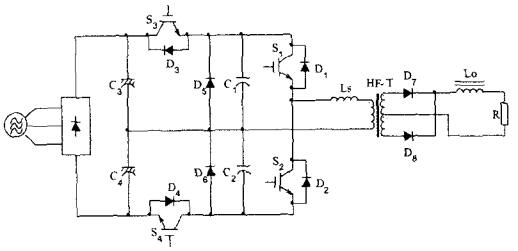


Fig. 5 Experimental Setup Circuit.

TABLE 1
DESIGN SPECIFICATIONS AND CIRCUIT PARAMETERS.

Item	Symbol	Value
Utility AC Input Voltage		400 [V]
Inverter switching Frequency	fs	40 [kHz]
Switching Period	Ts	25 [μs]
Leakage Inductance of HF Transformer	Ls	2 [μH]
Quasi Resonant Capacitor	C_1, C_2	0.235[μF]
Capacitance of DC smoothing Capacitor	C_3, C_4	2200[μF]
Inductance of DC Reactor in Load side	Lo	60[μH]
Load Resistance	R	0.09 [Ω]
Maximum Load current	Io	400 [A]
Turns Ratio of HFT	N_1:N_2:N_3	4:1:1

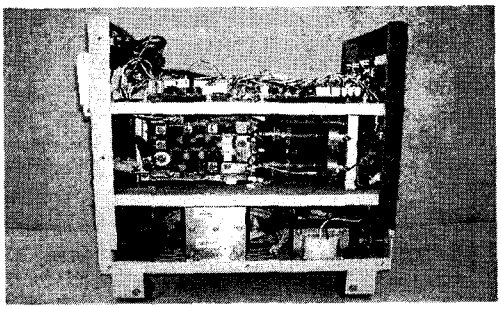
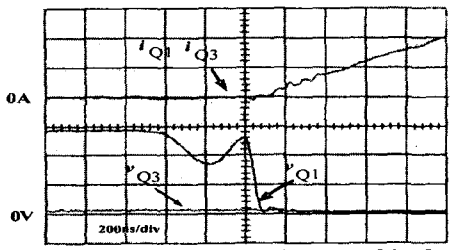


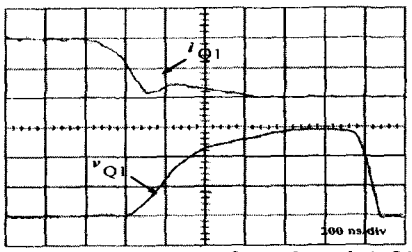
Fig. 6 Whole appearance of stick arc welding power supply using newly-developed soft switching dc-dc power converter.

B. Measured Switching Waveforms

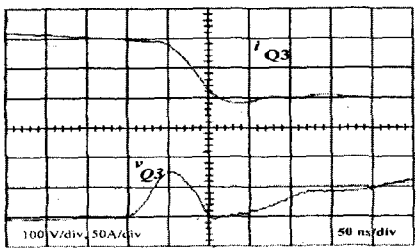
The switching operating waveforms for voltage and current when the switch Q_1 is turned on and turned off are shown in Fig. 7 (a) and (b). Observing these waveforms, the switch Q_1 is turned on with ZCS and is turned off with ZVS. The switching waveforms for voltage and current when the switch Q_3 is turned on and turned off are shown respectively in Fig 8. (a) and (c). Observing the operating waveforms, the switch Q_3 is turned on with ZVS/ZCS and is turned off with ZVS. However, at the turn-off transition for Q_1 and Q_3, some power loss still exists due to tail current characteristic of IGBTs.



Turn On switching waveforms for Q1,Q3



Turn off switching waveforms for switch Q1



Turn Off switching waveforms for Q3

Fig. 7 Measured switching voltage and current waveforms for active power switches Q_1 and Q_3

C. Comparative Results of Power Los Analysis

In power loss analysis and evaluations shown in Fig. 8, the total power loss of all the switches including Q_3 and Q_4 in newly-developed dc-dc power converter circuit is compared with that of all the switches in conventional hard switching PWM inverter type. The more the switching frequency of inverter increases, the more this newly-developed dc-dc power converter circuit has remarkable advantages as for the power conversion efficiency and power density as compared with the conventional hard switching dc-dc power converter.

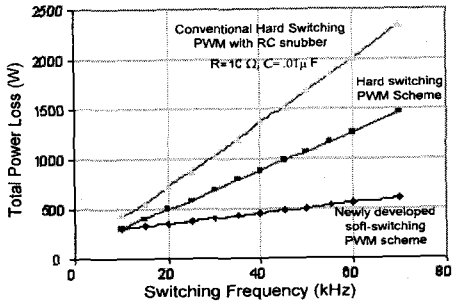


Fig. 8 Comparative power loss analysis between proposed soft switching PWM and conventional hard switching dc-dc converters.

V. CONCLUSIONS

In this paper, the novel circuit topology of half-bridge soft switching PWM dc-dc power converter with a high frequency link was presented. The operating principle and switching pattern of the half-bridge soft switching PWM dc-dc power converter described for 40 kHz, 36V, 400A output are illustrated and discussed for low voltage and large current output applications. The power loss analysis of the proposed soft switching power converter was discussed and evaluated as compared with hard switching PWM dc-dc power converter with a high frequency link. The practical effectiveness of the proposed dc-dc power converter operation under soft switching PWM scheme was actually proved from a practical point of view and the high efficiency and power density of this converter could be achieved on the basis of experimental results for Stick arc welder.

ACKNOWLEDGMENT

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