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Omega 형태의 게이트를 갖는 ZnO 나노선 FET에 대한 연구

김기현[1], 강정민[1], 윤창준[1], 정동영[2], 김상식[1*]
[1]고려대학교 전기전자전파공학과
[2]고려대학교 나노중점연구소

A study for omega-shaped gate ZnO nanowire FET

Kihyun Keem[1], Jeongmin Kang[1], Changjoon Yoon[1], Dong-Young Jeong[2], and Sangsig Kim[1*]
[1]Department of Electrical Engineering, Korea University
[2]Institue for Nano Science, Korea University

Abstract - Omega-shaped-gate (OSG) nanowire-based field effect transistors (FETs) have been attracted recently attention due to their highdevice performance expected from theoretical simulations among nanowire-based FETs with other gate geometries. OSG FETs with the channels of ZnO nanowires were successfully fabricated in this study with photolithographic processes. In the OSG FETs fabricated on oxidized Si substrates, the channels of ZnO nanowires with diameters of about 60 nm are coated surroundingly by Al_2O_3 as gate dielectrics with atomic layer deposition. About 80 % of the surfaces of the nanowires coated with Al_2O_3 is covered with gate metal to form OSG FETs. A representative OSG FET fabricated in this study exhibits a mobility of 98.9 cm^2/Vs, a peak transconductance of 0.4 μS, and an Ion/Ioff ratio of 10^6 the value of the Ion/Ioff ratio obtained from this OSG FET is the highest among nanowire-based FETs, to our knowledge. Its mobility, peak transconductance, and Ion/Ioff ratio are remarkably enhanced by 11.5, 32, and 10^6 times, respectively, compared with a back-gate FET with the same ZnO nanowire channel as utilized in the OSG FET

1. Introduction

The importance of gate geometry of semiconductor-based devices has been realized for the enhancement in device performance and for the integration for the past 10 years. In the developing trend of conventional metal-oxide-semiconductor field effect transistors (MOSFETs), planar MOSFETs have been developed to double-gate to tri-gate (FinFETs) MOSFETs. And, in the nanowire-based field effect transistors(FETs), back-gate FETs have been developed to cross-gate to top-gate FETs, although the back-gate nanowire-based FETs have still been fabricated mostly. From the both developing trends, the ideal gate geometry of both the conventional MOSFETs and the nanowire-based FETs is surrounding-gate FETs (SG FETs). Modeling and simulation for SG FETs widely studied for the past 10 years have demonstrated their high device performance. The fabrication of SG FETs were first achieved with Si/Ge shell nanowires by Lieber group[1], and vertical SG FETs with ZnO nanowires were subsequently fabricated by NASA group[2]. Nevertheless, only a few of SG FETs have been reported due to complexity of the fabrication of the SG FETs. Recently, simulation papers have proposed that omega-shaped-gate (OSG) field-effect transistors (FETs) exhibit similar device performances to SG FETs, in spite of their relatively simpler fabrication procedures. This proposal motivates our research on OSG FETs. Successful fabrication and high performance of OSG FETs with channels of ZnO nanowires are reported in this paper.

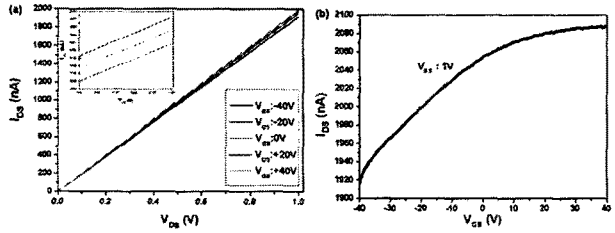
ZnO nanowires have been more attractive nanomaterials widely than other semiconducting nanowires due to their simple synthetic procedure, high crystalline quality, and electrical characteristics favorable to optoelectronics. These semiconducting nanowires grown by a variety of growth methods including thermal chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD), and pulsed laser deposition (PLD) are nearly defect-free single-crystallineand intrinsic low doping concentration due to their highly developed synthetic processes. Their electrical characteristics are significantly dependent on surface passivation, high-k dielectrics, and gate geometry. Recently, the enhancement of electron mobility (1000 cm^2/Vs) by polymer coating on the surface of ZnO nanorods has been reported by W. I. Park et al.[3] Passivation of ZnO nanorods by polymer coating suppresses interactions between surfaces of ZnO nanorod and molecular species, and carrier trappings or scatterings by surface defects. Applications of surrounding gate shape and high-k dielectrics such as self-assembled superlattice (SAS) improved device performance of ZnO nanowire-based FETs. SAS-based ZnO nanowire FETs exhibited a low operating voltage of 1.5 V[4], and surrounding-gate ZnO nanowire FETs exhibited the inversion characteristics of nanowire channel. These research results reveal the possibility that ZnO nanowires may be utilized for future high-speed electronic devices. In spite of the remarkable development in the ZnO-nanowire electronics, most ZnO nanowire-based FETs have still been based on back-gate ones, except the SG FET reported by a NASA group. In this study, OSG ZnO nanowire-based FETs with Al_2O_3 high-k dielectrics have been fabricated successfully with photolithographic processes Al_2O_3 dielectrics play roles not only as gate material but also as a passivation on the surface of the nanowire channel. Electrical characterization of the OSG ZnO nanowire-based FETs is performed, and their device characteristics are compared with those of back-gate FETs with ZnO nanowires

2. Results and discussions

For the fabrication of nanowire-based FETs in this study, some single-crystalline ZnO nanowires with a diameter of 60 nm were selected from ZnO nanowires grown on Si substrates by thermal CVD. Their cross section iscircular, their growth direction is perpendicular to the$(01\bar{1}0)$, and their averaged length is 70 μm.[5] Prior to the fabrication and characterization of OSG FETs, a representative back-gate FET with a channel of a single ZnO nanowire selected from the same sample as used for the OSG FETs was fabricated on a 300-nm thick oxide layer on the top of a Si substrate, and its electrical characteristics were investigated. In this back-gate FET, the electrodes were formed by thermal evaporation of Ti (30 nm) followed by Au (100 nm). The channel length between the electrodes is 6 μm. I_{DS}-V_{DS} curves taken for the back-gate FET are depicted in Fig. 1, revealing that their electrical properties are ohmic; in the inset of Fig. 1(a), magnified curves are added. The slope is not dependent significantly on gate voltage in a range from -40 to 40 V, although its dependence exhibitsthat the channel nanowire is n-type. A typical I_{DS}-V_{GS} curve obtained from the back-gate FET at V_{DS} of 1 V is plotted in Fig. 1b. The depletion is not seen in the range of gate voltage from -40 to 40 V, thereby an Ion/Ioff ratio is close to 1.09. And a peak transconductance (gm) is 12.5 nS at V_{DS}=1 V and at V_{GS}=-40 V. The field effect mobility is estimated to be 8.6 cm^2/Vs at V_{DS}=1 V on the basis of the formula of $\mu_{FE} = L_c L_g g_m / C_b V_{DS}$, where Lc is the channel length, Lg the gate length, and C the capacitance of the gate dielectrics. For the back-gate FET, Lc=Lg=6 μm. Capacitance is obtained to be 0.52 fF from the equation of $C_b \cong 2\pi\varepsilon_r\varepsilon_0 L_g / \ln(2h/r_{nw})$, where ε_r is the dielectric constant of SiO_2 (3.9), h the thickness of SiO_2 (300 nm), and rnw the radius of the nanowire (50 nm). For this back-gate nanowire-basedFET, the threshold voltage may not be estimated.

A top view of SEM image of an OSG ZnO nanowire-based

FET fabricated in our labis shown in Fig. 2(a). The cross-sectional TEM image taken for the OSG ZnO nanowire-based FET fabricated in this study is shown in Fig. 2(b). The cross-sectional TEM image reveals that the nanowire-based FET is indeed an omega-shaped one; the cross-sectional TEM image is tilted, so the scale bar is not added for avoiding confusion. The circular cross-section of the nanowire is coated by the Al_2O_3 layer and subsequently by Ti. About 80% of the surfaces of the nanowires coated with Al_2O_3 is covered with gate metal to form OSG FETs. The SEM and TEM images taken separately for the Al_2O_3 coated nanowire reveals that the diameter of the nanowire is 60 nm and that the thickness of the Al_2O_3 coated layer is 29 nm. Typical output and transfer characteristics obtained from a representative OSG ZnO nanowire-based FET with a channel length of 10 ㎛ and a nanowire diameter of 60 nm are shown in Fig. 3. The family of I_{DS}-V_{DS} curves (Fig. 3(a)) shows that drain current I_{DS} increases with drain voltage V_{DS}, and the straight form of the I_{DS}-V_{DS} curves exhibits ohmic contact. The slope of I_{DS}-V_{DS} curve increases dramatically as gate voltage V_{GS} varies from -6 to 10 V, compared with the back-gate FET. At V_{GS}=-6 V, the channel is depleted. The family of I_{DS}-V_{GS} curves in Fig. 3(b) shows that I_{DS} first increases and then saturates as V_{GS} varies from -5 to 10 V and is totally depleted in a V_{GS} range from -5 to -10 V. These characteristics reveal that the device is an n-type depletion mode FET.

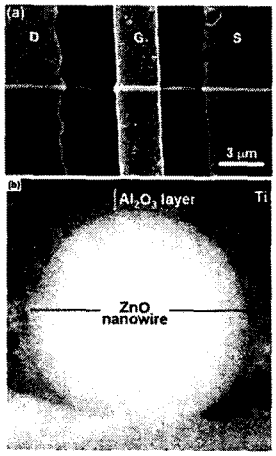


<Fig. 1> I-V characteristics of the back-gate ZnO nanowire-based FET. (a) I_{DS} vs. V_{DS} characteristics for different V_{GS} from -40 to +40 V. The inset shows their magnified characteristics. (b) I_{DS} vs. V_{GS} characteristics at V_{DS}=1 V

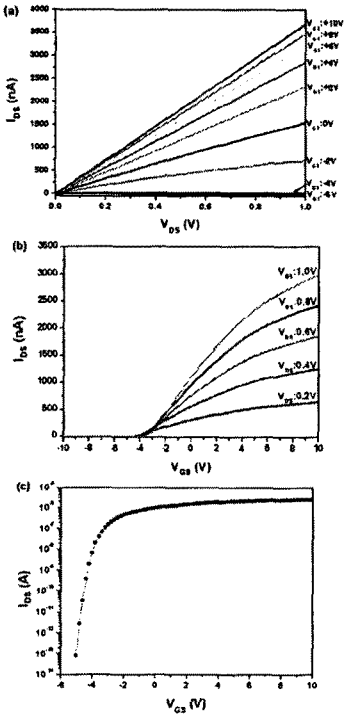
I_{DS}-V_{GS} transferand transconductance curves obtained from the representative OSG FET at V_{DS}=1 V are plotted in Fig. 3(c). The I_{DS}-V_{GS} transfer curve demonstrates an Ion/Ioff ratio of 10^6; the Ion/Ioff ratio is the highest among nanowire-based FETs, to our knowledge. Threshold voltage is obtained as -4.3 V from the I_{DS}-V_{GS} transfer curve. The subthreshold slope obtained from the I_{DS}-V_{GS} curves at V_{DS}=1 V yields a value of 130 mV/decade. Furthermore, the capacitance, electron mobility, and concentration of charge carrier for our OSG FETare estimated as follows. First of all, the capacitance C may be obtained to be 2.31 fF on the basis of the formulas $C_{omg} = 2\pi\varepsilon_r\varepsilon_0 L_g / \ln(r_g / r_{nw})$, where rg is the outer radius of the Al_2O_3 coated nanowire (59 nm), and ε_r is the dielectric constant of Al_2O_3 (9). The mobility is estimated to be 98.9 cm^2/Vs at V_{DS}=1 V using the formulas $\mu_{FE} = L_c L_g g_m r_g / C V_{DS} r_{nw}$, where Lc=10 ㎛, and Lg=3 ㎛. The concentration of charge carrier density is obtained to be 7.31×10^{18} cm^{-3} from the formulas $n_e = Q_{tot} / e\pi r_{nw}^2 L_g$, where $Q_{tot} = CV_{th}$. Field effect mobility, peak transconductance, and Ion/Ioff ratio are remarkably enhanced by nearly 11.5, 32, and 10^6 times, compared with the back-gate FET. The observed enhancement of the electrical characteristics is mostly attributed to the OSG geometry, the passivation of the surface of the nanowire by cladding of Al_2O_3, and the use of a higher-k dielectric Al_2O_3 material than SiO_2.

3. Conclusions

we havesuccessfully fabricated the OSG FETs with the channels of ZnO nanowires, and characterized their electrical characteristics. A representative OSG FET exhibits the remarkably enhancement of electrical characteristics, compared with a representative back-gate FET; the peak transconductance increases from 12.5 to 400 nS, the field effect mobility from 8.6 to 98.9 cm^2/Vs, and the Ion/Ioff ratio from 1.09 to 106. The observed enhancement of the electrical characteristics is mostly attributed to the OSG geometry, the passivation of the surface of the nanowire by cladding of Al_2O_3, and the use of a higher-k dielectric Al_2O_3 material than SiO_2.



<Fig. 2> (a) The top view of SEM image of the OSG FET fabricated by photolithographic process (b) Cross-sectional TEM image of the OSG FET.



<Fig. 3> Electrical characteristics of omega-shaped gate ZnO nanowire FET

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