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수소이온주입 도즈량 및 어닐링 조건에 따른 dislocation 밀도 변화에 대한 고찰

Effect of Hydrogen Implantation Dose and Annealing Condition on Dislocation Density

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Beyond 60nm C-MOS FET's needs fully depleted SOI C-MOS FET fabricated on nano-Silicon on Insulator (SOI) substrate those silicon thickness becomes less than 20nm. Electron and hole mobility degraded if the silicon thickness for nano SOI is less than 20nm because of carrier confinement in the device channel inversion region (called as quantum effect) C-MOS FET's fabricated on strained Si-on-Insulator (sSOI) sSOI's are produced by hydrogen implantation, bonding between device (strained Si/graded SiGe/ Si substrate) and handle wafer (SiO_2/Si substrate), cleavage annealing, and surface smoothing However, it's shown the cross-hatch & dislocation on the growing SiGe layer for fabricating sSOI wafer In this study, it is estimated the cross-hatch pattern & dislocation after the growth of graded SiGe layer on Si substrate by UHV-CVD to increase from 20% to 30% of Ge concentration It's measured the density of them to implant hydrogen slightly beyond the interface between Si-substrate and SiGe layer and anneal the nitride ambience as well as changing the dose and the annealing time. *This work was financially supported by Korea Ministry of Science & Technology through the NRL program