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SOI wafer Pseudo MOS Transistor 에서의 SOI 및 BOX Thickness 에 따른 trap density 의 종속성

Dependency of SOI & BOX Thickness on trap density of SOI wafers in Pseudo MOS Transistor

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Pseudo-MOS transistor is being considered a powerful technique to evaluate the trap density at the interface between Si and buried oxide layer of SOI wafer, because it is not necessary to fabricate any device process In pseudo MOS transistor, the quality of SOI wafers can be characterized by calculation of trap density at interface between top Si and berried oxide layers via measuring I-V & C-V characteristic curves through a four point probes In the paper, we investigated trap densities from several SOI wafers such as SIMOX, SUMCO and SOITEC We found that the trap density increased with decreasing SOI & buried oxide thickness, and the drain current of pseudo-MOS transistor was decreased with increasing a channel length In addition, we concluded that bonded SOI wafers showed less trap density than SIMOX SOI