Low Cost FPGA-based Control Strategy for a Single Phase Stacked Multicell Converter

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ABSTRACT

Multilevel converters have emerged like a new strategy for energy conversion from medium power to high power. The main characteristic of the topologies classified as multilevel, is the use of commutation devices connected in series, allowing the distribution of the voltage and reducing stress in the commutation switches. Stacked Multicell Converter (SMC), is classified as single-phase voltage source inverter (VSI). Due to the fact, the SMC generates a signal of alternating current of several levels of voltage of direct current. The following work will demonstrate the flexibility of the above mentioned topology using a low cost control circuit architecture.

1. INTRODUCTION

A Stacked Multicell Converter is a topology derived from Multicell Converters. Therefore, many of the multicell converters characteristics apply for the Stacked Multicell Converter [1-3]. Figure 1 shows a multicell converter. This converter is made up basically of p pairs of switches of three quadrants separated by p-1 floating voltage sources, and it is fed by an input voltage E. Each pair of switches referenced as (Ak, Bk) with k ∈ [1....p], is known as basic commutation cell [3, 4].

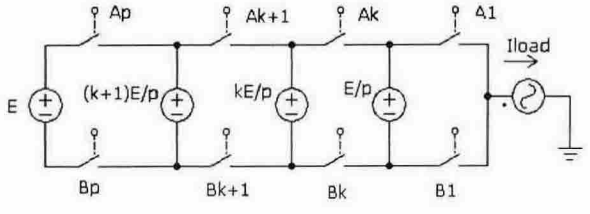

Fig. 1 Multicell Converter

The blocking voltage of each commutation cell is given by:

$$(k+1)\cdot\frac{E}{p}-k\cdot\frac{E}{p}=\frac{E}{p} \qquad (1)$$

The commutation cells are functional only if the floating voltage sources do not provide average power. This can be solved if these sources are replaced by capacitors, which require that the current becomes zero in every period of commutation [4-6].

2. STACKED MULTICELL CONVERTER

A SMC of pxn is designed by n rows (stacks), and p columns produced by the association of commutation cells. The number of synthesized voltage levels depends on the amount of commutations that constitute the structure. For example, for a pxn converter, it is possible to obtain (pxn)+1 output voltage levels, including the zero volt level.

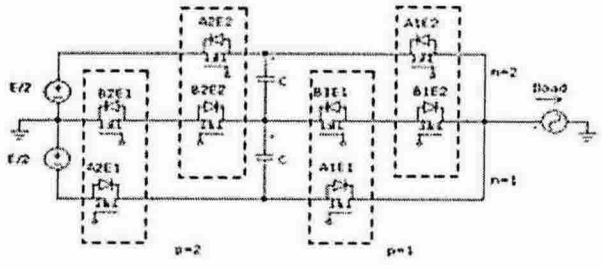

Fig. 2 2x2 Stacked Multicell Converter

Thus, capacitor voltage in each cell is equal to:

$$V_{ck}=\frac{kE}{pxn} \qquad (2)$$

The applied voltage of each commutation cell (Vcell), is given by capacitor voltage difference [5]:

$$V_{cellk}=V_{ck+1}-V_{ck}=\frac{(k+1)E}{pxn}-\frac{kE}{pxn}=\frac{E}{pxn} \qquad (3)$$

3. CAPACITOR VOLTAGE BALANCE

For a 2x2 SMC, it is possible to guaranteed that the maximum voltage for each switch will not be greater than *E/pxn*. Consequently, the current that flows through capacitor Ck can be expressed like a function of the control signals applied to both adjacent cells, thus:

$$i_{Ck}(t) = (D_{k+1} + I(t) - D_k(t)) \cdot I_{Sw} \qquad (4)$$

Where:

$D_k(t)$=1 when A(i+1Ej) is turned on.

$D_k(t)$=0 when A(i+1Ej) is turned off.

Equation 4, gives the voltage stability condition in steady state for Vck (k=1, 2,..., p-1); so, to obtain a power-flow control between both sources is necessary that the floating voltage sources do not provide average power, and therefore can be deducted that:

$$\int_0^T (D_{k+1} + I(t) - D_k(t))dt = 0 \qquad (5)$$

Of which, we can infer that:

$$\Rightarrow D_1 = D_2 = \cdots D_p = D \qquad (6)$$

It is possible to deduce that the stability condition is satisfied as soon as the control signals have the same duty cycle. Therefore, the power balance occurs during both parts of the period. When switch A(i+1Ej) is conducting, and therefore exists a current that flows through Ck that indicates absorbed energy. On the other hand when A(1+1Ej) is off exists a current that flows through Ck of negative order what suggests the capacitor is providing energy [6-8].

4. HORIZONTALLY PHASE SHIFTED CARRIER PWM CONTROL STRATEGY

In the practice, the global modulation is used to create n-secondary modulation signals, each of these define the state of each row. In this case, the modulating signals come from each p stage of the SMC structure and the carrier signal is delayed by 360°/p. For the specific case of the 2x2 structure, each carrier signal is delayed by 180°.

The implementation of the control system, based on horizontally phase-shifted carrier PWM, uses the integrated circuit DSP MCD330 from Analog Devices and the ALTERA's FPGA [9].

The signals for the control generation. have a frequency of 60Hz, modulated at 20 kHz with a maximum duty cycle of 80% (fig. 3).

Twelve signals are generated simultaneously from the DSP, which accomplish the adjacent-same row cells out-of-phase firing sequence. An experimental prototype was implemented to validated the control system, a 2x2 SMC with an input voltage E of 300V (fig. 4).

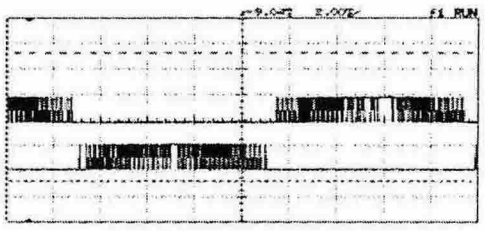

Fig. 3 DSP control signal (Time/Div=2ms)

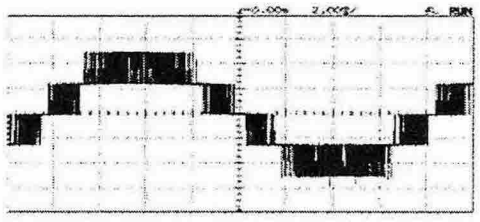

Fig. 4 Experimental results (Output Voltage ; 20V/Div)

It is clear that the capacitors voltage is balanced, the property of natural balancing is directly inherited from the classical multicell structure [10]. The two flying capacitors voltage for the converter are both equal to about 75 V after balancing. As is observed, the previous control shows that the natural voltage balance in the capacitors is feasible and the output waveform has a clean shape. However the cost of generate such waveform depends mainly on the DSP and the support devices and components needed.

5. SIMPLE SWITCHING CONTROL STRATEGY

In order to obtain a permanent signal, a state sequence should be generated continuously. Applying a positive voltage and allowing the necessary states sequence for the three levels, it is possible to obtain the positive part of the alternating signal. To obtain the output voltage, an exact timing in each architecture block should be precise. Both characteristics are found in a FPGA. Thus, the ALTERA's FPGA 303ALC44-10 is selected and implemented with the MAX II+PLUS software to generate the firing sequences [9, 11]. To synthesize output sine wave, the pattern pulses for a 2x2 SMC must be a 3 level 60Hz output signal over a 60kHz

base switching signal. The permanence of the states in the 3 level 60Hz output signal is based on dividing the time required (in this case 16.666ms), in a proportional sine wave shape.

Reconstructing the signal, the desired output voltage waveform must be as in figure 5.

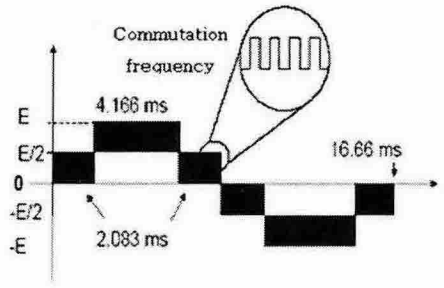

Fig. 5 60 Hz output waveform

In order to assemble the signal of 60Hz, is required that the voltage levels adapts much as possible to this waveform. Starting with the transition between level 0 and $E/2$ during exactly 2.083ms., afterward the transition between $E/2$ and E during 4.166ms., and finally, transition between $E/2$ and level 0. In the case of the negative levels is just to use the desired negative levels.

The results of the experimental waveform for a signal of 60Hz are shown in figure 6, this result is obtained from a 300Vdc (E) input voltage and resulting on a output voltage signal of 150Vac. In figure 6 observe an unequal output voltage signal for the transition levels between 0 and $E/2$ and $E/2$ and E. This unbalance is produced by the capacitors' charge-discharge cycles [3, 9]. But in the other hand if the timing necessary (same duty cycle on control signals), for this charge-discharge cycle do not accomplish the stability condition (eq. 5), the natural capacitor process (balance), will not be achieved giving by result an unbalanced output voltage signal as shown in figure 6. With this control philosophy is demonstrated that is possible to synthesize a sinusoidal signal with this architecture by means of simple switching, but the consequence of this simple control type causes unbalanced voltage effects in the store energy elements [7, 8].

6. CONCLUSION

The presented analysis demonstrates the flexibility of the SMC on the basis of a simple circuit control strategy. The importance of a right control strategy to preserve the natural balancing of energy on the passive components of this architecture is mandatory if a right circuit behavior is desired. The storage components in every circuit should be designed with precautions due to the fact as more energy stored less efficient and more expensive design. By other hand, due to the number of semiconductors, is possible to improve the quality of the generated current using low-cost low-power devices.

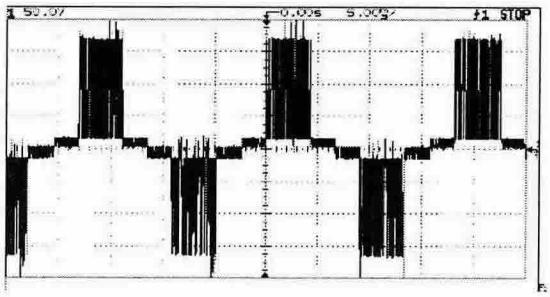

Fig. 6 Result of the experimental waveform of 60Hz of switching frequency

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