간단한 전류원 형태의 구조를 갖는 새로운 PDP 에너지 회수 회로

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A simple energy recovery circuit with current-fed type for plasma display panel (PDP)

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Abstract

High efficiency and low cost sustain driver for plasma display panel (PDP) with current fed is proposed. Main concept of the proposed circuit is using the current source to charge and discharge panel. As a result, all power switches can achieve the zero voltage switching (ZVS) and every auxiliary switch can also do the zero current switching (ZCS). Moreover, since the inductor current can compensate the discharge current, the current stress of all power switches can be reduced considerably. Furthermore, it has features as a simpler structure, less mass, less cost, and lower electromagnetic interference than prior circuit.

1.Introduction

The plasma display panel (PDP), invented at the University of Illinois in 1946 by Prof. Bitzer and Prof. Slottow, is praised for its large screen size, wide viewing angle, long life, high contrast ratio, thinness and etc. Therefore, it is obvious that PDP is the best candidate for high-definition television (HDTV) with high resolution. Fig. 1 shows simplified structure of PDP with three electrodes. It consists of two glass plates filled with chemically stable rare gases , helium (He) or xenon (Xe) and it comprises transparent X and Y sustain electrodes covered with a dielectric layer on the face plate, address electrodes perpendicular to the sustain electrodes on the back plate. A desired color can be realized by exciting the phosphors on the addressing electrode to emit visible light with the ultraviolet photons generated by gas discharge. [1]

Generally, the PDPs have been driven with the address display separation (ADS) method. The Operation of driving is divided into three periods of reset, addressing, and sustaining periods as shown Fig 2. During the reset period, a high voltage (usually larger than 340V) is forced between X electrode and Y electrode to initialize on all the cells in order to obtain a same condition for all the cells. In the addressing period, wall charges are accumulated in cells which make image to be displayed. In last period, sustaining, the discharges occur in cells addressed previously and the desired image can be obtained in panel.

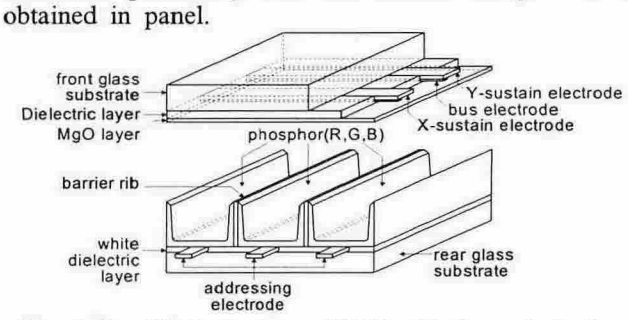

Fig. 1 Simplified structure of PDP with three electrodes.

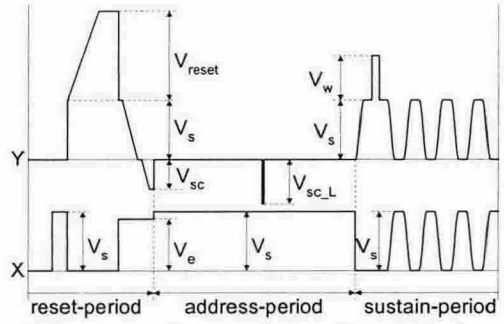

Fig. 2 Voltage waveform applied to X and Y electrodes in ADS driving method

During sustaining period of Fig. 2, panel voltage waveform is rectangular pulse from V_S to $-V_S$ between electrode X and Y. Due to the existence of dielectric layer, PDP is purely capacitive load (C_P) in respect to circuit operation. As a result, during charging and discharging transients, $2C_PV_s^2$ of energy is consumed for one cycle where CP and VS are the panel capacitance and the power supply voltage, respectively. If operating frequency is defined by f, then the total consumed energy becomes $2fC_PV_S^2$ [2]. If the operating frequency f and VS is increased, unusable energy is considerable and causes the serious problems in driving PDP. In addition, the surge current for charging and discharging transient intervals cause electromagnetic interference (EMI)

noise.

To solve these problems, the sustain driver with energy-recovery-circuit (ERC) is essential in sustaining period to display desired image effectively in PDP. Therefore, many energy recovery circuits have been proposed [3-9]. Among them, energy recovery circuit using LC resonant concept [3-4] features high efficiency and good circuit flexibility to cope with various driving methods. Therefore a number of leading PDP maker have adopted this circuit. In addition, several researchers have investigated various new circuits to improve performance and reduce circuit volumes. But there are some drawbacks such as low efficiency, bulk size, manufacturing or limitation of high frequency driving.

Therefore, in this paper, a new sustain driver with energy recover circuit of PDP is proposed to solve drawbacks of prior circuits with new driving concept of current fed. The proposed circuit builds up the inductor current before inverting the polarity of the panel. As a result, the main power switches are turned on under zero voltage condition and the auxiliary switches are turned off under zero current condition. Furthermore, since the inductor current compensates the discharging current, the current stress of main power switches can be considerably reduced. In addition, the proposed sustain driver shows high efficiency and EMI noise resulting from no surge current. Since the transient time can be shortened, PDP can be driven in high frequency to obtain high luminance efficiency.

2. The Proposed Energy Recovery Circuit

2.1 Operational Principles of the Proposed energy recovery circuit Circuit

Fig. 3 shows the circuit diagram and key waveform of the proposed energy recovery circuit for PDP. The proposed energy recovery circuit features that simpler structure, less mass and lower cost for production because it has only two auxiliary power switches and two inductors instead of bulky additional circuit for ERC as shown Fig 3 (a). The operation of the proposed energy recovery circuit can be divided into two half cycles, t0~t4 and t4~t8, and mode diagrams are shown in Fig. 4. Because the operation of two half cycles are symmetric, only the first half cycle is considered.

Mode 1($t_0 \le t \le t_1$): In this mode, since the switches, M3 and M4, are turned on and other switches are turned off, the panel voltage, v_{Cp}, is sustained to VS by turned on switches, M1 and M2.

Mode 2($t_1 \le t \le t_2$): When an auxiliary switch M5 is turned on at t1, mode2 begins. During this mode, inductor current, both i_{L1} and i_{L2}, are built up linearly with slope of $V_s/(L_1+L_2)$ through M3, M4, M5 and body diode D6 of M6. But the panel voltage is still maintained to V_s by turned on switches, M1 and M2. The current is expressed as:

$$i_{L1}(t) = i_{L2}(t) = \frac{V_s}{2L}(t - t_1) \quad (1)$$

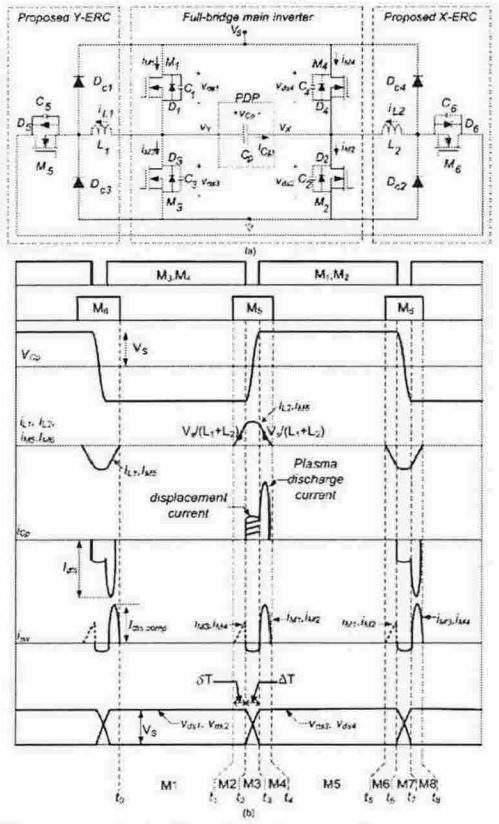

Fig. 3 The proposed circuit and its key waveforms
(a) Circuit diagram of the proposed circuit (b) Key waveforms

Mode 3($t_2 \le t \le t_3$): When M3 and M4 are turned off with M5 on state, mode 3 begins at t2. Since and the series resonant circuit is formed by $L_1=L_2=L$ and C_P with initial conditions of $v_{ds1}(t_2)=v_{ds2}(t_2)=V_s$, $v_{ds3}(t_2)=v_{ds4}(t_2)=0V$, $v_{Cp}(t_2)=-V_s$ and $i_{L1}(t_2)=i_{L2}(t_2)=(V_s/2L)\delta T$, the panel voltage, $v_{Cp}(t)$, and displacement current of C_P , $i_{Cp}(t)$ are given by

$$v_{Cp}(t) = -V_s \cos\omega_c(t-t_2) + \sqrt{\frac{2L}{Cp}}\left(\frac{V_s}{2L}\delta T\right)\sin\omega_c(t-t_2) \quad (2)$$

$$i_{Cp}(t) = \left(\frac{V_s}{2L}\delta T\right)\cos\omega_c(t-t_2) + \sqrt{\frac{C_p}{2L}}(V_s)\sin\omega_c(t-t_2) \quad (3)$$

where $\delta T=t_2-t_1$ and $\omega_c=1/(2LC_P)^{0.5}$. Before t_3, v_{Cp} is clamped to V_S and the output capacitors of switches, M1 and M2, are discharged. Therefore, the voltage across M1 and M2 falls to zero.

Mode 4($t_3 \le t \le t_4$): When switches, M1 and M2, are turned on at t3 under zro voltage condition, mode 4 begins and t iL1(+)flows to the input source through body diode D1 of M1 and iL2(+) also flows through body diode D2 of M2 and two inductor current is decreased with slope of $-V_s / (L_1+L_2)$. The inductor current is given by:

$$i_{L1} = i_{L2} = i_{L2}(t_3) - \frac{Vs}{2L}(t - t_3) \quad (4)$$

It is noted that this results in the canceling of the

panel discharge current in M1 and M2simultaneously. Due to compensating panel discharge current in the main power switches, the current stresses on the power switches M1 and M2 can be greatly reduced as shown Fig. 5 (b). During this mode, the compensated current of the main inverter switches can be expressed as

$$i_{M1}(t) = i_{M2}(t) = i_{dis,comp}(t) = i_{dis}(t) - i_{L1}(t) \quad (5)$$

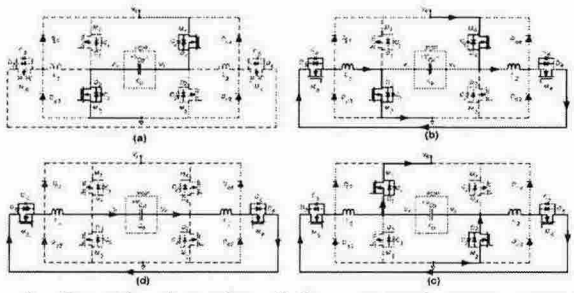

Fig. 4 Operational modes of the proposed energy recovery circuit. (a) Mode 1 (t0~t1) (b) Mode 2 (t1~t2) (c) Mode 3 (t2~t3) (d) Mode 4 (t3~t4)

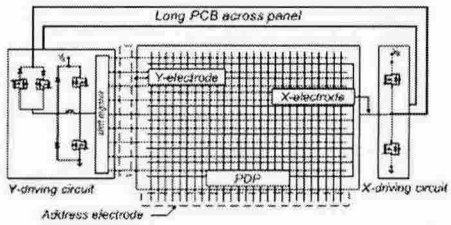

Fig. 5 Long PCB across panel to apply the parallel resonant type in industrial PDP.

The auxiliary switch is turned off when the inductor current becomes zero at t_4. During mode 4, the panel voltage, V_y, is sustained to V_S.

The circuit operation of t4~t8 is similar to that of t_0~t_4. Therefore the operation is repeated. In the circuit diagram, there are diodes, D_{C1}~D_{C4}, are used to clamp the voltage of auxiliary switches to V_S when they are turned off.

mode 2, the energy-recovery inductor has sufficient energy so that panel voltage, V_x and V_y, can go up to the sustain voltage V_S or go down to $-V_S$. Moreover, during mode 3, the conduction losses of the main inverter switches can also be reduced significantly and the current stresses of the main inverter switches can be reduced due to inductor current compensating discharge current. In addition, the switches, M1 and M2 are turned on in zero voltage condition and the auxiliary switch M5 are turned off in zero current condition. Therefore, the high efficiency can be obtained with simple ERC method because of canceling discharge current and soft switching of power switches.

2.2 Features of the proposed energy recovery circuit

The proposed energy recovery circuit can be applied to drive the large screen size with the fast transition time and high frequency. To obtain these features, it is very important to select the value of inductance for energy recovery operation.

Table 1. Inductance value to obtain desired transition time in the prior circuit and the proposed circuit where C_p=80nF (42-inch PDP)

	Series resonant type	Parallel resonant type	Proposed sustain driver
Transition time ΔT	$2\pi\sqrt{LC_p}$	$\pi\sqrt{LC_p}$	$\sqrt{2LC_p}\left[\sin^{-1}\left(1/\sqrt{(\delta T/\sqrt{2LC_p})^2+1}\right)+\theta\right]$ [1]
Inductor for ΔT = 600ns	0.227 μH	0.455 μH	1 μH when built-time, δT = 200ns
Inductor for ΔT = 500ns	0.158 μH	0.306 μH	1 μH when built-time, δT = 300ns
Inductor for ΔT = 400ns	0.100 μH	0.200 μH	0.7 μH when built-time, δT = 300ns

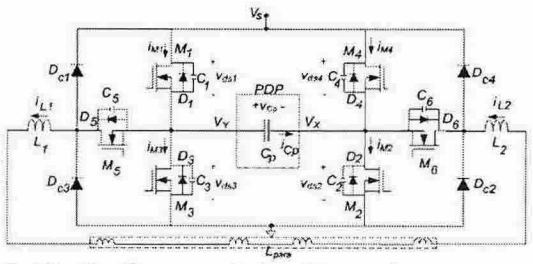

Fig. 6 Circuit diagram of the improved energy recovery circuit to overcome problem of the parasitic inductor on wire across panel

It is noted that, during In section 3.1, two prior circuit using resonance between panel capacitance, Cp, and resonant inductor, L, are studied. As shown in Table 1, if two prior circuit are applied to 42-inch PDP (Cp=80nF), the series resonant type circuit [3] needs two inductors with inductance of 0.227uH and the parallel resonant type [4] needs inductor with value of 0.445uH to obtain the transition time of △ T=600ns. If the board has some parasitic inductor, the two prior circuits cannot achieve the desired fast transition time. Therefore, the faster the transition time is, the harder inductor is designed as shown in table 1. However, the proposed energy recovery circuit with two inductors of value of 1uH can be applied to 42-inch PDP and can obtain the sufficient transition time. In other word, it is insensitive to the effect of parasitic components. And, the parallel resonant type needs too long wide PCB conductor across panel to reduce the parasitic inductor value as shown in Fig.5. This means that it is hard to obtain normal operation due to parasitic inductor on the wire. Therefore, it is hard to use the parallel resonant type to the industrial PDP. Although the proposed driver seems to be similar to parallel resonant type, it can be applied to industrial PDP. The improved energy recovery circuit can be obtained without additional circuit as shown in Fig. 6. By replacing auxiliary switches by two inductor, the inductors can absorb the parasitic inductance with same operation of the proposed energy recovery circuit.

3. Design considerations

It is assumed that the parasitic components, such as resistor, inductor and etc are neglected because the normal operation is not affected by parasitic components. The transition time △T is defined as the time duration which the panel voltage is changed from $-V_S$ to V_S . By replacing t-t_1 to &T and $v_{Cp}(t)$

to V_S, the equation (4) becomes:

$$V_s = -V_s \cos \omega_c(\Delta T) + \sqrt{\frac{2L}{C_p}}\left(\frac{V_s}{2L}\delta T\right)\sin \omega_c(\Delta T) \quad (6)$$

By solving this equation, $\triangle T$ can be obtained when δT is defined as the time duration which the inductor current is built up before the inversion of the panel polarity. As a result, the transition time $\triangle T$ can be given by

$$\Delta T = \sqrt{2LCp}\left[\sin^{-1}\left(1/\sqrt{(\delta T/\sqrt{2LCp})^2+1}\right)+\theta\right] \quad (7)$$

where $\theta=\tan^{-1}((2LC_p)^{0.5}/\delta T)$. The transition time, $\triangle T$, is decreased as the current build-up time δT is longer with fixed value of $L_1=L_2=L$. This means that another design factor is considered in designing inductor L. It means that if the faster transient time is wanted with fixed inductance, the more inductor current should be built up before transition.

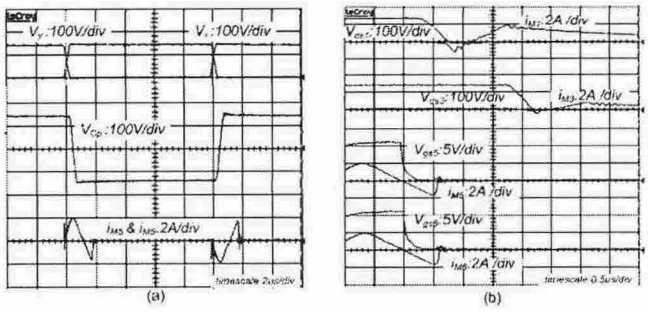

Fig.7 Experimental waveforms of the proposed energy recovery circuit (a)Voltage Waveforms of X,Y node, VCp and current waveforms of iM5 and iM6 (b)Turn on transient waveforms of M1 and M3 and turn off transient waveforms of M5 and M6

4. Experimental Results

A prototype energy recovery circuit for PDP is implemented with specifications as follows: $L_1=L_2=L=2uH$, $C_p=2nF$ (6 inch panel), M1-M6=2SK2995, clamp diodes=S20LC30, gate driver IC=IR2110, switching frequency=50kHz, transition time $\triangle T \leq$ 800ns, and V_S =141V. Fig. 7 shows the experimental results of the proposed circuit. The panel voltages Vx and Vy are charged and discharged from VS to 0V and from 0 to V_S respectively, without voltage notches. In Fig.7 (a), during the built-up interval, V_{Cp} is sustained and auxiliary switch current (inductor current) increases linearly, and after the reversing polarity of panel, they are recovered. Fig.7 (b) shows that the output capacitors of switches are discharged fully when power switches are turned on. This means that all main inverter switches are turned on in zero voltage condition In addition, the auxiliary switches are turned off in zero current condition. As it can be shown in experimental waveform, the proposed circuit employed current-injection method has advantages of full charging and discharging of panel, and therefore, soft-switching of power switches. Furthermore, the number of device is less and the structure of circuit is simpler than those of the prior circuit.

5. Conclusion

A new current-injection PDP energy recovery circuit has been proposed to overcome drawbacks of the prior circuits. This circuit features a simpler structure, lower cost of production, etc. Moreover, the main power switches are turned on under zero voltage condition and the auxiliary switches are turned off under zero current condition. Therefore, it shows higher efficiency and lower EMI noise. Furthermore, since the panel discharge current is compensated, it shows low current stress and low conduction loss. In addition, it enables to light for the panel without consideration effects of the parasitic components. And also, the proposed energy recovery circuit can be designed easily without considering the parasitic components and can promise fast transient time $\triangle T$ according to value designed. Therefore, the proposed circuit is expected to be very suitable for the energy recovery circuit of the high-definition PDP TVs.

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References

[1] Hirakawa, H., Katayama, T., Juroki, S., Nakahara, H., Nanto, T., Yoshikawa, K., Otsuka, A. and Wakitani, M.: 'Cell structure and driving method of a 25-in (64 cm) diagonal high resolution color AC plasma display', Proc. S.I.D.,1988,29, pp. 279-282

[2] Webber, L.F.: 'Measurement of wall charge and capacitance variation for a single cell in AC plasma display panel', IEEE Tran. Electron Devices, 1997,24,(7), pp. 864-869

[3] Webber, L.F. and Wood, M.B.: 'Energy recovery sustain circuit for the AC plasma display', S.I.D., 1987, pp 92-95

[4] M. Ohaba and Y. Sano: 'Energy recovery driver for a dot matrix ac plasma display panel with a parallel resonant circuit allowing power reduction', U.S. Patent 5 670 974, Sep, 1997

[5] S. K. Han, J. Y. Lee, G. W. Moon and M. J. Youn : "Cost-Effective Energy Recovery Display Driver for 42-inch Plasma Display Panel", IECON'04 , pp. SA2-2 Nov. 2004, Busan. Korea

[6] S. K. Han, S. W. Choi, G. W. Moon and M. J. Youn: "Zero-Voltage and Zero-Current Switching Energy Recovery Circuit for Plasma Display Panel", PESC'04, pp. 782-786, 20-25 June. 2004 Aachen, Germany

[7] S.K. Han, G. W. Moon, and M. J. Youn: "Current-fed energy-recovery circuit for plasma display panel", Electronics Lett. pp 1035-1036 Vol. 39 No. 14 10th July 2003

[8] S.Y. Lin, C.L.Chen, and K. Lee, "Novel regerative current feds for plasma display panel", in Proc. IEEE PESC'98, Fukuoka, Japan, 1998, pp. 1739-17433.

[9] H.B. Hsu, C.L. Chen, S. Y. Lin, and K. M. Lee, "Representative power electronics driver for plasma panel in sustain mode operation". IEEE Trans. Ind. Electron, vol. 47, pp 1118-1125, Oct. 2000.

[10] J.Y. Lee, J.S. Kim, N.S. Jung, and B. H. Cho "The current injection method for AC Plasma Display Panel(PDP) Sustainer", IEEE Trans. Ind. Electronics, vol. 51, NO. 3 pp 615-624, June, 2004