Low-Voltage Current Feed-back Amplifier

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Abstract: This paper proposed the new current feed-back amplifier for low supply voltage application. The input stage was designed to be a class-AB circuit and achieve the low supply-voltage operation down to $2V_{TH}+2V_{DS(SAT)}$. With the self-adjust bias current, the high performance can be adopted with high stability. The circuit was successfully proven by the simulation with MOSIS 0.5 μm MOS technology.

Keywords: Low-voltage circuit, Current Feed-back Amplifier, Analog Circuit.

1. INTRODUCTION

Current Feedback Amplifiers (CFA) fundamentally different architecture and offers significant performance advantages over the traditional the Voltage Feedback Amplifier (VFA). The CFA was proved in a increasing of slew rate and a bandwidth that is relatively independent of the closed loop gain, and be traded-off DC precision [1]. The greater of slew rate leads to faster rise/fall times and less intermodulation distortion [2-3]. To take the most benefit of this kind of circuit, motivate to low voltage design for portable and/or wireless device, such as mobile phone.

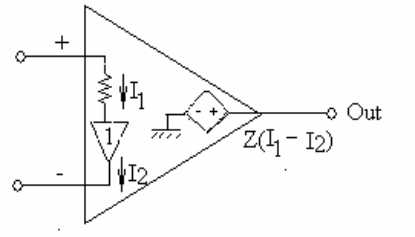
Figure 1(a) shows the idealized model of CFA. In conventional design, a unity gain buffer is connected between the two input terminals (+ and -) that forced the inverting terminal (-) to have a same voltage of non inverting terminal (+). This unity gain buffer ideally has zero output impedance and infinite input impedance. As a result, the inverting input impedance is zero whereas the non-inverting input impedance is infinite. The current difference, then feed through current-controlled voltage source with zero output impedance to drive the output stage to inversely track the V_{in} with the gain configured by feedback network.

The conventional CFA is shown in fig.1 (b). The transistor pair (M1-M2) and (M3-M4) are formed in the unity gain buffer which are biased with I1 and I2, respectively. For the large supply voltage, M1 and M3 are always on and working in complimentary fashion. The output currents of unity gain buffer ($I_{ds(M2)}$ and $I_{ds(M4)}$) then copied to high gain stage (M9-M10) and output stage (M11-M12), consequently.

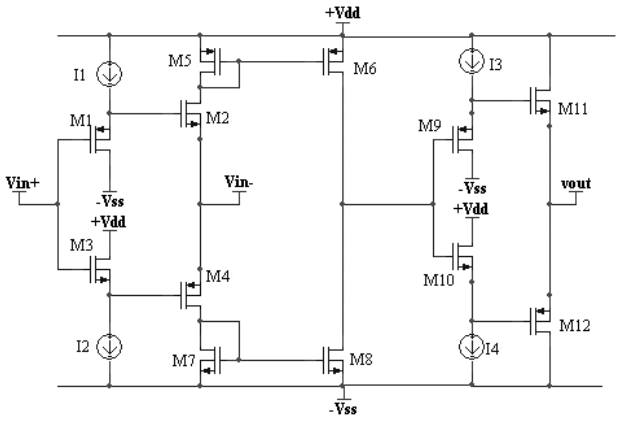
Unfortunately, this conventional circuit is not proper for low voltage design due to the large voltage required at the input stage (the unity gain buffer). This paper proposed the new low voltage CFA which the input stage is designed in folded-cascode class-AB style, that details in section two. The simulation result and conclusion can be found in the two last sections.

2. LOW-VOLTAGE CURRENT FEEDBACK AMPLIFIER (LVCFA)

Figure 2 show the proposed CFA, the transistor pairs (M1-M2) and (M3-M4) are formed the folded-cascode unity gain buffer which biased with self-biasing current loop (M5-M8). Assuming the PMOS and NMOS threshold voltage are close and equal V_{th}. Therefore,



(a)



(b)

Fig.1 (a). Ideal-CFA (b). Conventional-CFA

$$I_1 = \frac{\beta_p}{2}(V_{dd} - V_{in}^{+} - V_{th})^2$$

and $$I_2 = \frac{\beta_p}{2}(V_{in}^{+} - V_B - V_{th})^2 \quad (1)$$

$$I_1' = \frac{\beta_n}{2}(V_A - V_{in}^{+} - V_{th})^2$$

and $$I_2' = \frac{\beta_n}{2}(V_{in}^{+} - V_{ss} - V_{th})^2 \quad (2)$$

The current mirror (M5-M6) and (M7-M8) force ($I_1' = I_1$) and ($I_2' = I_2$), respectively.

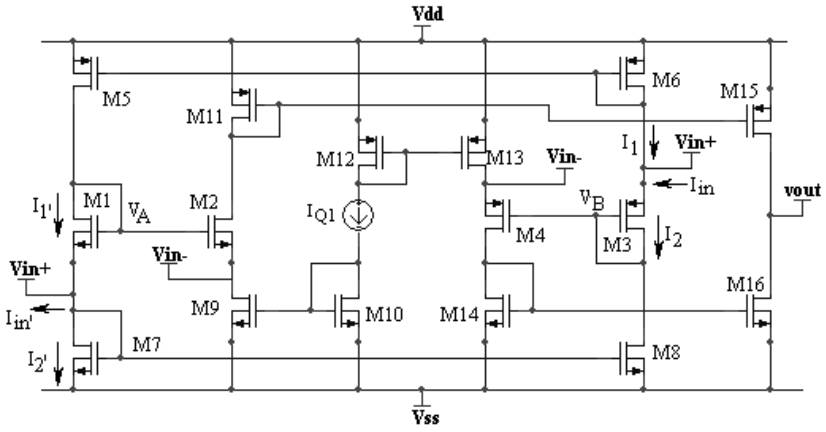


Fig.2 Proposed LVCFA

$$V_A = (V_{in}^{+} + V_{th})\left(V_{dd}\sqrt{\frac{\beta_p}{\beta_n}} - 1\right) \quad (3)$$

$$V_B = (V_{in}^{+} - V_{th})\left(V_{ss}\sqrt{\frac{\beta_n}{\beta_p}} + 1\right) \quad (4)$$

The input current can be found as follow

$$I_{in} = I_2 - I_1 \quad \text{and} \quad I_{in}' = I_1' - I_2' \quad (5)$$

For large supply voltage

$$(|V_{dd} - V_{ss}| > 2V_{th} + V_{ds(sat)} + V_{in(swing)}),$$

all transistors are operate in saturation region. From current loops and eq.1, the input current and V_{in}^{+} terminal is equal $2I_{in}$.

On the other hand, the low supply voltage

$$(|V_{dd} - V_{ss}| \le 2V_{th} + V_{ds(sat)} + V_{in(swing)}^{+}),$$

it force the circuit to operate in class-AB mode. When ($V_{in}^{+} > V_{dd} - V_{th}$), M5-6 are driven to operate in sub-threshold region and the small current (I_1 and I_1') now present as a quotient current (I_Q) in class-AB operation. At this time, M3 and M7-8 still operate in saturation region and yield the V_B follow the eq.4. In the same way, when ($V_{in}^{+} < V_{th} - |V_{ss}|$), M7-8 are operate in sub-threshold region, while as, M1 and M5-6 are in saturation region and follow the eq.3.

The biasing network (M9-10 and M12-13) with small quotient current (I_{Q1}), try to maintain the M11 and M14 to operate in class-AB mode. The simplified version of output stage is formed by M15-16.

3. SIMULATION AND RESULT

The proposed circuit is design with the MOSIS 0.5um transistor model. The dual supply voltage (V_{dd} and V_{ss}) that use in this paper, are 0.75V and -0.75V, respectively. Table.1 lists all transistors size. Finally, I_{Q1} set to be 10uA and 20k-ohm resistive load (R_{load}) is used in all simulation.

Table 1 Aspect ration of the proposed FCFA (L=0.5um).

TR	W(um)	TR	W(um)
M1	4	M9	5
M2	4	M10	5
M3	25	M11	15
M4	25	M12	15
M5	15	M13	15
M6	15	M14	5
M7	5	M15	360
M8	5	M16	90

A. Non-inverting amplifier

Fig.3 shows the non-inverting amplifier. By setting the R_G to be 1k and vary R_F (1k, 5k, 7k, 10k and 20k-ohm) results the amplifier gain (0.3, 0.8, 1, 1.3 and 2.5, respectively. The dc-characteristic results show in fig.4.

Two kinds of input signal, sinusoidal and square ware, are used to verify the transient response. By setting the input signal at 10 and 100MHz, fig 5(a) and (b) show the simulation result of unity gain non-inverting amplifier (R_F = 7k-ohm) with $\pm$ 0.2V sinusoidal and $\pm$ 0.1V square-wave input signal, respectively. Fig.6 shows the frequency response of unity gain non-inverting amplifier and cut-off (-3dB) at 140MHz.

B. Inverting amplifier

Fig.7 shows the inverting amplifier diagram. All parameter setting are same as previous circuit (non-inverting amplifier). Fig.8 shows the inverting amplifier dc-characteristic by setting R_G(1k) and vary R_F to (1k, 3k, 7k and 20k-ohm) that results the circuit gain (-0.85, -4, -5.5 and -13.5), respectively

Fig.9 show the transient responses of inverting amplifier with gain = 2, by setting R_G (1k) and R_F (2.7k-ohm) with $\pm$ 0.2V input signal. The cut-off frequency (-3dB) is 218MHz that show in fig 10.

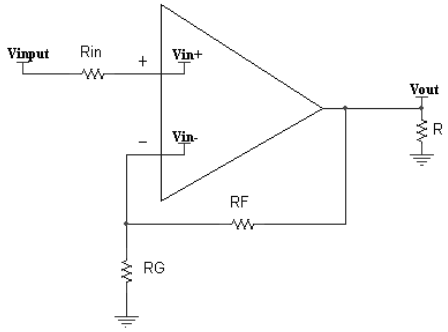


Fig.3 Non-inverting amplifier

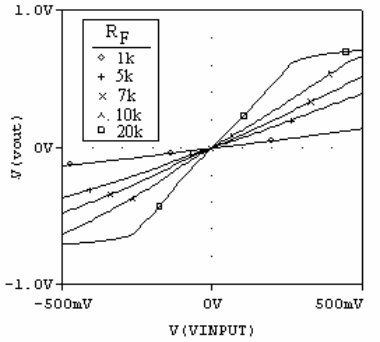
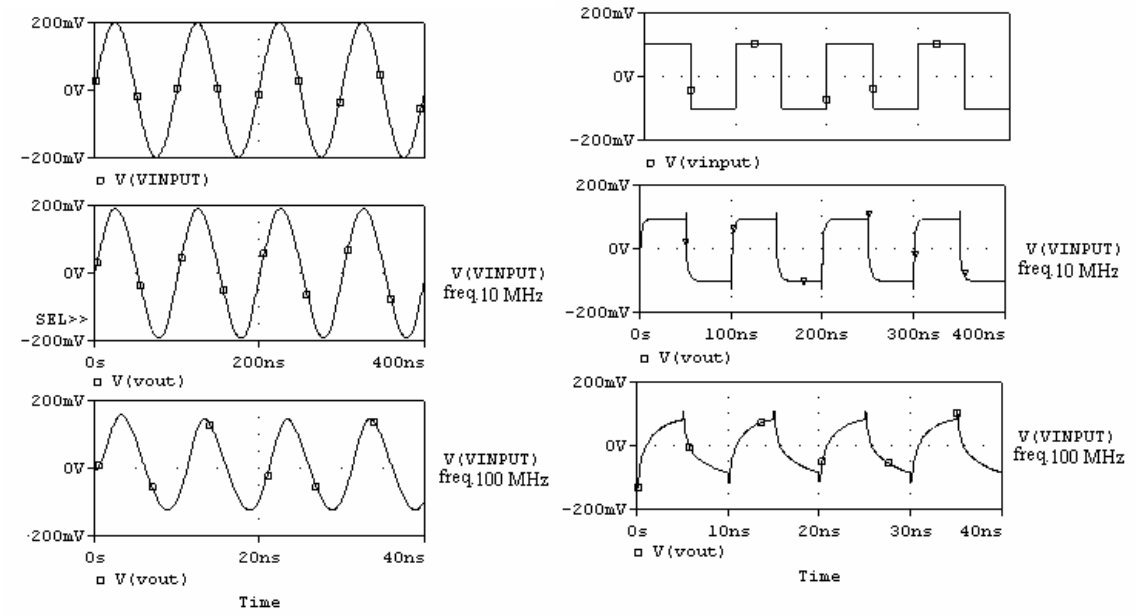


Fig.4 Non-inverting amplifier dc-characteristic



(a) (b)

Fig.5 Transient response of non-inverting amplifier
(a) sinusoidal input (b) square-wave input

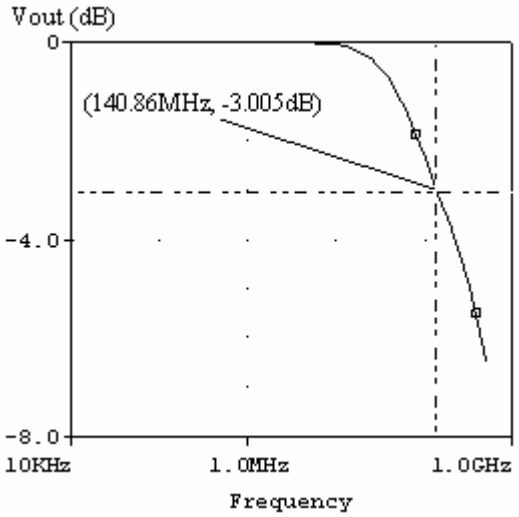


Fig.6 Frequency response of non-inverting amplifier

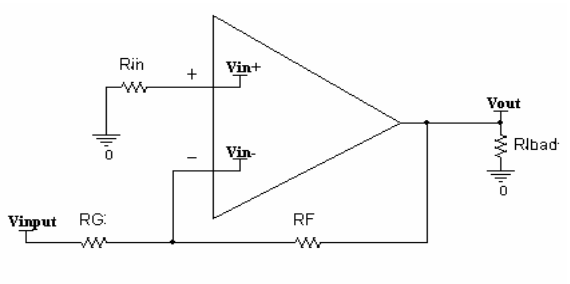


Fig.7 Inverting amplifier

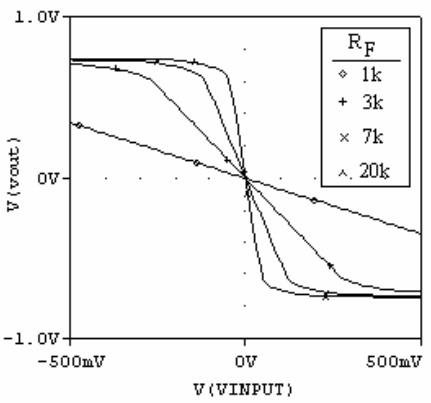


Fig.8 Inverting amplifier dc-characteristic

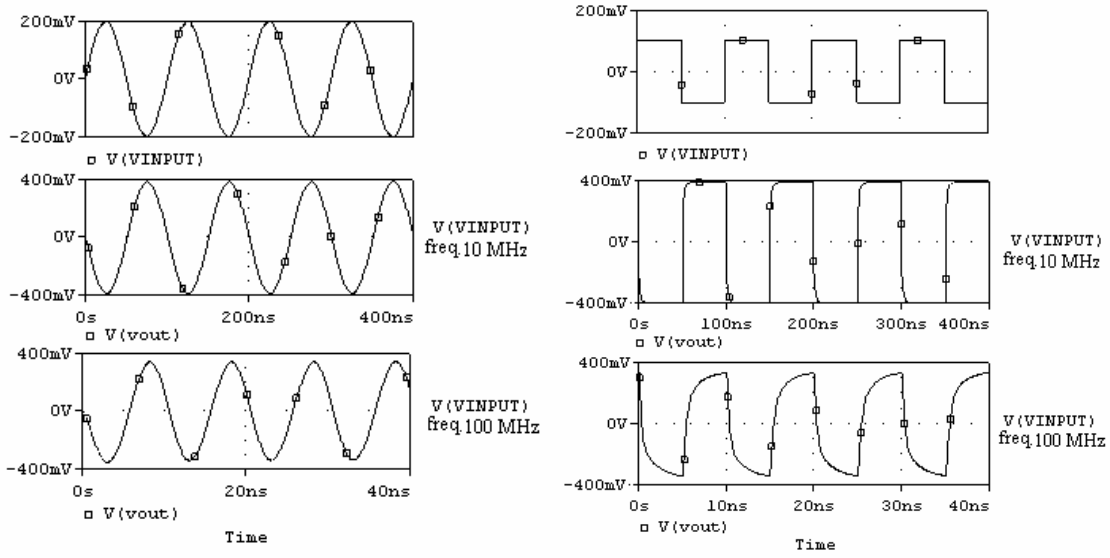


Fig.9 Transient response of inverting amplifier
(a) sinusoidal input (b) square-wave input

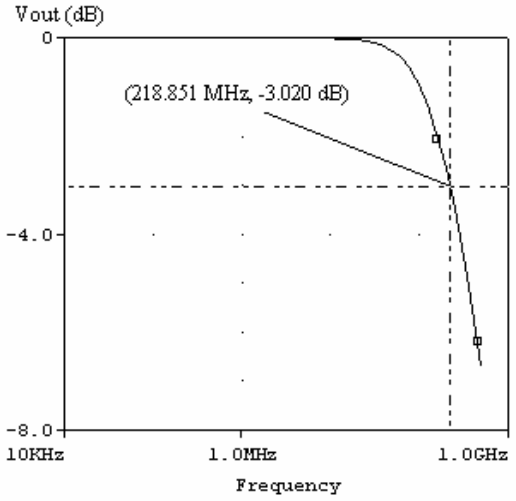


Fig.10 Frequency response of inverting amplifier

4. CONCLUSION

The low voltage current feedback that purposed in this paper, simulation results have shown the excellent performance with high stability and wide bandwidth. The high slew rate of CFAs is much faster than Voltage feed backs leads to faster rise/fall times that make this circuit applicable to mixed-signal processing.

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