A High Efficiency Power Supply with High Power Factor Input

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Abstract—This paper presents a single-stage ZVT full-bridge AC/DC converter for aerospace applications. The detailed operating principle and design consideration of this soft-switched converter are analyzed and described. The proposed circuit topology and control scheme are proposed to exhibit optimum performances (i.e. high power factor, high efficiency, ring-free and low EMI features). A laboratory prototype, 500W 5V/100A AC/DC converter was implemented. The simulation and experimental waveforms verify the feasibility of the proposed design.

Keywords— Single-Stage, Soft-Switched Converter, Current-Doubler Synchronous Rectification, Ring-Free, EMI

I. Introduction

Mechanically steered antennas switch slowly between satellites in aerospace applications. The electronic phased array system (PAS), including a 1500-element antenna, permits fast redirection between satellites for high data-rate retrieval applications. As shown in Fig. 1, the PAS antenna requires a $5V_{DC}/100A$ power supply [1]. The phase-shifted zero-voltage transition (ZVT) full-bridge DC/DC converter, shown in Fig. 2, is the most commonly used soft-switched topology in high power applications such as aircraft power systems, telecommunications and medical electronics [2-4]. The zero voltage turn-on range of the primary switches can be extended to light load condition by intentionally increasing the transformer leakage and external inductances. However, the parasitic ringing generated by the large transformer leakage / external inductances and transformer stray capacitance causes additional losses and EMI problems [5, 6]. The widely used center-tapped diode rectifier in Fig. 2 has one nearly constant diode drop in high current path, which causes over 50% power loss and limits the conversion efficiency in low voltage / high current applications [7, 8]. Table 1 shows the current harmonic specifications for a commercial aircraft power system. To comply with the stringent requirements, the commonly used approach is to cascade a power factor correction (PFC) circuit in front of the DC/DC converter as shown in Fig. 2. Such a two-stage structure presents low efficiency and high complexity. This research is focused on the reduction of current harmonics, parasitic ringing, and secondary rectification losses with simple topology. A single-stage ZVT full-bridge AC/DC converter with a ring-free mechanism is combined with a current doubler synchronous rectifier to produce optimum performance including high power factor, high efficiency, ring-free and low EMI features for PAS power system applications. A modified phase-shifted control method is proposed to regulate the output voltage of this single-stage converter. In the following sections, the operating principles and control design will be discussed in detail. The simulation and experimental results from a laboratory prototype are given to show the feasibility of the proposed scheme.
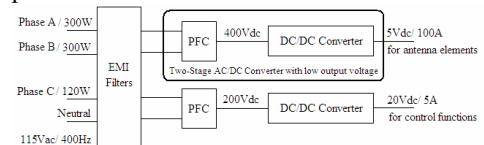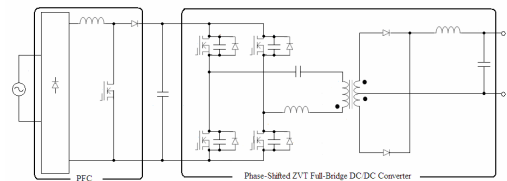

Fig. 1 The conventional PAS power supply

Fig. 2 The conventional two-stage AC/DC converter

II. Circuit Operation

The circuit topology of the proposed single-stage AC/DC converter is shown in Fig.3. Q1 and Q2 operate as the lagging-leg primary switches while Q3 and Q4 operate as the leading-leg primary switches. The PFC and the DC/DC cells share the power switch Q2. The input inductor, L_{in} is designed to work in discontinuous conduction mode (DCM). D1~D4 and C_{p1}~C_{p4} are the anti-parallel diodes and parasitic capacitances of the primary switches, respectively. A fast-recovery diode, D_{in} is placed in cascade with the input inductor to prevent circulating current through D2 and D4. C_{dc} represents the DC bus capacitor and C_b is a blocking capacitor that prevents flux imbalance in the transformer core. The resonant inductance L_r represents the sum of the transformer leakage inductance L_l and external inductance L_e. The addition of two ring-free diodes Da and Db is to eliminate the parasitic ringing phenomenon caused by the resonant inductor and stray capacitor of transformer winding. SR1 and SR2 act as the synchronous switches on the transformer secondary side. DS1 and DS2 are the body diodes of the corresponding synchronous switches. To fully benefit from synchronous rectification, the conduction criteria for the synchronous switches SR1 and SR2, replaces the corresponding body diodes (DS1 and DS2) conduction in the high current path. A modified phase-shifted control method is used to regulate the output voltage of this single-stage AC/DC converter.
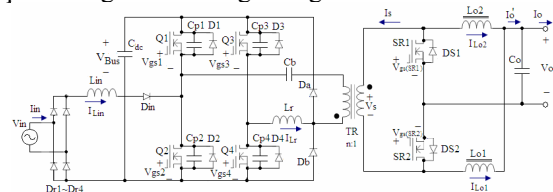

Fig. 3 The proposed single-stage AC/DC converter for low voltage/ high current output applications

Based on the symbols and signal polarities introduced in Fig. 3, the theoretical waveforms of the proposed converter are shown in Fig. 4. Referring to the equivalent circuits in Fig. 5, the detailed operating principles of the proposed converter are explained as follows:

Mode 1(t0~t1): The power switches Q1 and Q4 remain turned on, the current that flows through the resonant inductor L_r and the primary winding of power transformer is equal to $-I_{Lo1}/n$, the first output inductance current I_{Lo1} referred to on the primary side. Corresponding synchronous switch SR1 conduction ensures that the output rectification losses are low. The current I_{Lo1} of the first output inductor L_{o1} flows through SR1 and the transformer secondary winding, closing the loop through the output capacitor C_o. The current I_{Lo1} ramps up linearly while I_{Lo2} ramps down linearly. The transformer secondary winding carries only approximately half of the output current and ripple currents cancelled on common output capacitor C_o.

Mode 2(t1~t2): Q4 is turned off at t1, the freewheeling current I_{Lr} starts to charge C_{p4} and discharge C_{p3}. Thus, the drain to source voltage V_{ds4} across the power switch Q4 increases and the drain to source voltage V_{ds3} across the power switch Q3 decreases.

Mode 3(t2~t3): Until t2 the decreased voltage V_{ds3} falls to zero, the voltage on both the primary and secondary windings become zero. The freewheeling current I_{Lr} keep flowing through the anti-parallel diode D3 of the power switch Q3 to ensure the zero voltage turn-on for Q3.

Mode 4(t3~t4): As long as the power switch Q3 is turned on at t3 before the inductor current I_{Lr} changes its direction, zero-voltage switching can be assured. Corresponding synchronous switch SR2 conduction ensures that the output rectification losses are low. The current Io' freewheels through the synchronous switches SR1 and SR2. The voltage across L_{o1} also becomes negative, and equals the output voltage amplitude. Therefore the current I_{Lo1} ramps down like the current I_{Lo2}.

Mode 5(t4~t5): When Q1 is turned off at t4, the resonant inductor L_r starts to resonate with the parasitic capacitances C_{p1} and C_{p2} of the power switches Q1 and Q2. The resonant current I_{Lr} starts to charge C_{p1} and discharge C_{p2}.

Mode 6(t5~t6): Until t5 the decreased voltage V_{ds2} falls to zero and the DC bus voltage forces the inductor current I_{Lr} to start commutation.

Mode 7(t6~t7): As long as power switch Q2 is turned on before the inductor current I_{Lr} changes its direction at t6 and zero-voltage switching can be assured. Thus, the ZVS conditions for the power switch Q2 can be determined as follows:

$$T_{d,max} \le \frac{L_r I_{Lr}(t5)}{V_{Bus}} + \frac{\pi}{2}\sqrt{L_r(C_{p1} + C_{p2})}, \qquad (1)$$

$$L_r \ge (C_{p1} + C_{p2}) \times \left(\frac{V_{Bus}}{I_{Lr(t3)}}\right)^2, \qquad (2)$$

On the secondary side, synchronous switch SR1 is turned off and the freewheeling current flows through the corresponding body diode DS1. During this interval, the DC bus voltage remains to force the inductor current I_{Lr} increasing. At t7, I_{Lr} is equal to I_{Lo2}/n, the second output inductance current referred to on the primary side. The body diode DS1 of synchronous switch SR1 is then released.

Mode 8(t7~t8): The inductor current I_{Lr} starts to charge the stray transformer winding capacitor. The resonance caused by inductor L_r and the stray capacitor could be clamped while the ring-free diode Da is conducted. The current I_{Lo2} of the secondary output inductor L_{o2} flows through SR2 and the transformer secondary winding, closing the loop through the output capacitor C_o. The current I_{Lo2} ramps up linearly while I_{Lo1} ramps down linearly. When Q2 is zero-voltage turned on, the voltage across the input inductor L_{in} is equal to the rectified input voltage $|V_{in}|$ such that the input inductor current I_{Lin} increases linearly.

Modes 9~12(t8~t12): At t8, Da is released due to the inductance current I_{Lr} stays at I_{Lo2}/n. During modes 9~12, the zero-voltage-switching for the power switch Q4 can be also achieved as similar as modes 1~4. In this interval, the input inductor current $|I_{Lin}|$ remains to increase linearly.

Modes 13~16(t12~t16): When the drain to source voltage V_{ds2} across the power switch Q2 increases and then the voltage across the input inductor L_{in} decreases to zero, the input inductor current, I_{Lin} reaches its peak. Assuming AC sinusoidal source voltage $V_{in}(t)=V_m\sin(2\pi f_i t)$ and the dead-time interval is enough short to be negligible, the peak input inductor current, $I_{Lin(peak)}$ of each switching cycle can be expressed as

$$I_{Lin(peak)} = \frac{|V_m \sin(2\pi f_i t)|}{2 f_s L_{in}}, \qquad (3)$$

where f_s is the switching frequency and f_i is the line frequency. When Q1 is zero-voltage turned on and SR2 is turned off, the resonance caused by inductor L_r and the transformer stray capacitor could be clamped while the ring-free diode Db is conducted. The voltage across the input inductor L_{in} is equal to $(|V_{in}|-V_{bus})$ such that the rectified input current $|I_{Lin}|$ decreases linearly and finally reaches zero at t17. The circuit will then proceed back to mode 1 after completing one operating cycle T_s.
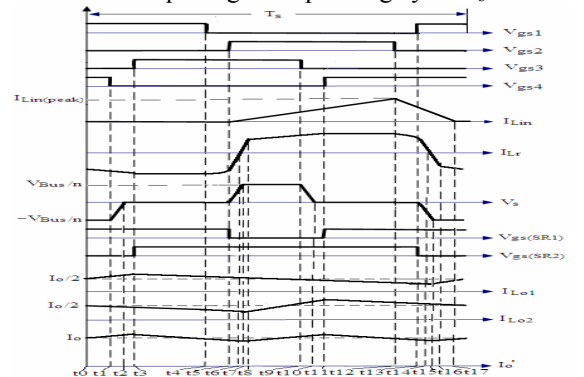

Fig. 4 Theoretical waveforms of the proposed AC/DC converter

Mode 1 (t0~t1)	Mode 2 (t1~t2)
Mode 3 (t2~t3)	Mode 4 (t3~t4)
Mode 5 (t4~t5)	Mode 6 (t5~t6)
Mode 7(t6~t7)	Mode 8 (t7~t8)
Mode 9 (t8~t9)	Mode 10 (t9~t10)
Mode 11 (t10~t11)	Mode 12 (t11~t12)
Mode 13 (t12~t13)	Mode 14 (t13~t14)

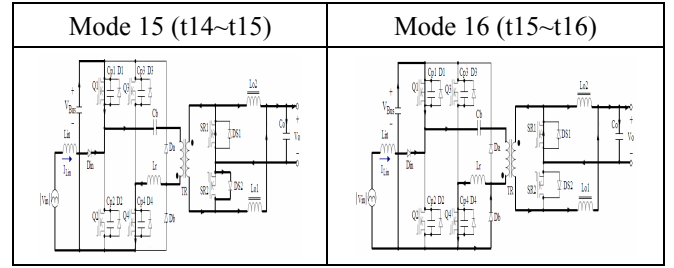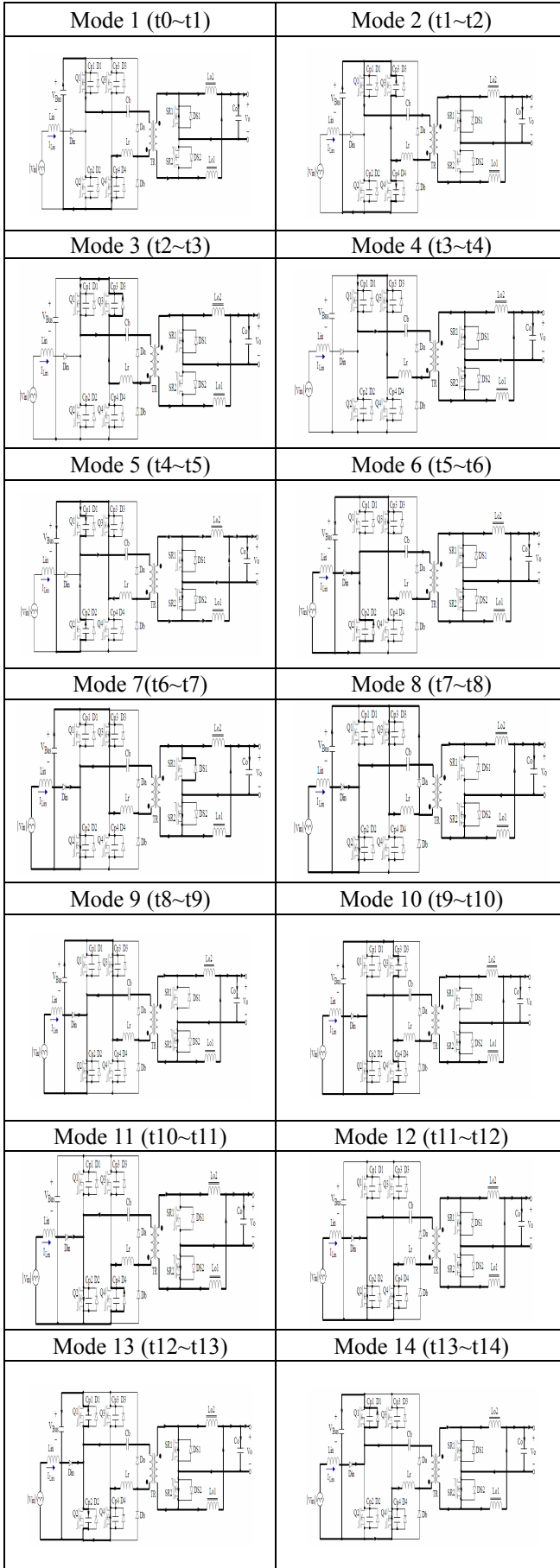| Mode 15 (t14~t15)	Mode 16 (t15~t16)

Fig. 5 Equivalent circuits for different switching modes

III. Steady-State Analysis

In following analysis, the dead-time interval is assumed negligible. The output inductors are operated in the continuous conduction mode (CCM) and are large enough so that current ripples on them are negligible. When the two diagonally placed primary switches (either Q1 and Q4 or Q2 and Q3) keep conducting during active interval δT_s, energy is transferred from the input voltage source through the corresponding conducting synchronous switch (SR1 or SR2) to the load. The source current can be shaped automatically to follow the source voltage by designing the input inductor to operate at DCM. With phase-shifted control, the gating signal for power switch, Q2 always has a 50% duty cycle. The average input inductor current, $I_{Lin(on)}$ during on-time of Q2 and the average input inductor current, $I_{Lin(off)}$ during off-time of Q2 can be expressed as follows:

$$I_{L_{in}(,on)} = \frac{|V_{in}|}{8f_s L_{in}}, \tag{4}$$

$$I_{L_{in}(,off)} = \frac{V_{in}^2}{8f_s L_{in}(V_{Bus} - |V_{in}|)}, \tag{5}$$

The expressions for the average input inductor current, $I_{Lin(av)}$ of each switching cycle and the average input power, $P_{in(av)}$ are as follows:

$$I_{L_{in}(,av)} = \frac{|V_{in}|}{8f_s L_{in}} \frac{M_{PFC}}{M_{PFC} - |\sin(2\pi f_i t)|}, \tag{6}$$

$$P_{in(av)} = \frac{1}{2\pi} \int_0^{2\pi} (|V_{in}| \times I_{Lin(av)}) d\theta$$

$$= \frac{1}{2\pi} \int_0^{2\pi} (|V_{in}| \times I_{Lin(av)}) d\theta d\theta$$

$$= \frac{V_m^2}{4\pi f_s L_{in}} \int_0^{\pi/2} \left(\frac{M_{PFC} \sin^2 \theta}{M_{PFC} - \sin \theta}\right) d\theta, \tag{7}$$

$$M_{PFC} = \frac{V_{Bus}}{V_m}, \tag{8}$$

where M_{PFC} is the voltage transfer ratio of the PFC cell at peak input voltage, V_m. The output power, P_o can be represented by Equation (9). In steady-state, the output power P_o should be equal to the average input power $P_{in(av)}$. Thus, the voltage transfer ratio $M_{AC/DC}$ of the proposed single-stage AC/DC converter can be expressed as Equation (11).

$$P_o = \frac{V_o^2}{R_L}, \tag{9}$$

$$M_{DC/DC} = \frac{V_o}{V_{Bus}} = \frac{\delta}{n}, \quad (10)$$

$$M_{AC/DC} = \frac{V_o}{V_m}$$

$$= \sqrt{\frac{R_L}{4\pi f_s L_{in}} \int_0^{\pi/2} (\frac{M_{PFC} \sin^2 \theta}{M_{PFC} - \sin \theta}) d\theta}, \quad (11)$$

where R_L is the load resistance of the AC/DC converter.

IV. Design Considerations

A. Control Design

A modified phase-shifted control method is used to regulate output voltage of the single-stage AC/DC converter. Figure 6 shows a schematic diagram of the proposed control circuit. The phase-shifted PWM control signals can be produced using commercialized control ICs, such as UC3879. The voltage regulation for the DC/DC cell can be achieved by varying the phase-shift between the two legs of the bridge circuit. However, the gating signal for power switch, Q2 always has a 50% duty cycle. The DC bus voltage in the proposed single-stage AC/DC converter cannot be regulated by conventional phase-shifted control method. Based on Equation (7), a variable frequency control circuit then is added to vary the input power of PFC cell by adjusting the switching frequency. The power balance for the single-stage AC/DC converter can be achieved by regulating the DC bus voltage as shown in Fig. 6. A DC bus protection circuit was also implemented. When the voltage feeding back from the DC bus reaches the upper voltage, V_U, the power switch Q2 is turned off to protect the DC bus until the feedback voltage is less than the lower voltage, V_L. Synchronous switches SR1 and SR2 can be controlled by using self-driven and external-driven methods. The merits of the self-driven configuration are ease of implementation and fewer components. However, the critical drawback of large variation in $R_{ds(on)}$ depending on operating conditions does exist [9, 10]. To fully benefit from synchronous rectification, the external-driven approach was adopted and the conduction criteria for the synchronous switches SR1 and SR2 involves replacing the corresponding anti-parallel diodes DS1 and DS2 in the high current path. The control logic for synchronous switches SR1 and SR2 can be determined from 16 combinations of switching states as shown in Table 2, where "1" represents turned-on, "0" represents turned-off and "x" means neutral. When the synchronous switch state is marked neutral, this state will not occur in a practical circuit. However, the switch can still be logically turned off without affecting the circuit operations. If we replace "x" in the Table 2 with "0", the look-up table dimensions can be greatly reduced. From Table 2, the gating signals for SR1 and SR2 can be derived and simplified as follows:

$$SR1 = \overline{Q2 \cdot \overline{Q4}}, \quad (12)$$

$$SR2 = \overline{Q1 \cdot \overline{Q3}}, \quad (13)$$

In practical implementation, SR1 (SR2) must be turned off before V_s goes from zero to the positive (negative) level in order to avoid a current spike through the transformer winding and both SRs, causing unnecessary power loss. When V_s goes from positive (negative) level to zero, SR1 (SR2) will remain off until Q4 (Q3) is turned on to avoid the shoot-through. The simulation waveforms are shown in Fig. 7(a) to verify the feasibility of the proposed gating logic for the synchronous switches.

B. Inductor Design

Based on the design criteria proposed in [12], the input inductor L_{in} must satisfy the condition as follow:

$$L_{in} \leq \frac{0.48(M_{PFC} - 1)^2}{(M_{PFC} - 0.92)M_{PFC}^3} \frac{R_{in(DC/DC)}}{2f_s}, \quad (14)$$

where $R_{in(DC/DC)}$ is the equivalent input resistance of the DC/DC cell. From Equation (9), we can obtain the equivalent input resistance $R_{in(DC/DC)}$ for the DC/DC cell:

$$R_{in(DC/DC)} = \frac{\eta_{(DC/DC)} R_L}{M_{DC/DC}^2}, \quad (15)$$

where $\eta_{(DC/DC)}$ is the efficiency of the DC/DC cell. Combining (14) and (15), we can determine the input inductor L_{in}.

$$L_{in} \leq \frac{0.48(M_{PFC} - 1)^2}{(M_{PFC} - 0.92)M_{PFC}^3} \frac{\eta_{(DC/DC)} R_L}{2f_s M_{DC/DC}^2}, \quad (16)$$

As previously mentioned, when two primary switches on the same side of the bus trail (either Q1 and Q3 or Q2 and Q4) keep conducting during the passive interval $(1-\delta)T_s$, the transformer windings are shortened due to conduction in the synchronous switches (SR1 and SR2). The proposed current doubler synchronous rectifier shown in Fig. 7(b) can be equivalent to Fig. 7(c) during these passive intervals. Thus, the relationship between output current ripple $\Delta I_{o(pk-pk)}$ and equivalent output inductor L_{eq} can be expressed by:

$$\Delta I_{o(pk-pk)} \leq \frac{(1-\delta)V_o}{f_{s(min)} L_{eq}}, \quad (17)$$

$$L_{eq} = L_{o1} // L_{o2}, \quad (18)$$

where $f_{s(min)}$ is the minimum switching frequency of the primary switches. For the given output current ripple specification, the output inductors L_{o1} and L_{o2} can be realized with the same inductance L_o and determined by:

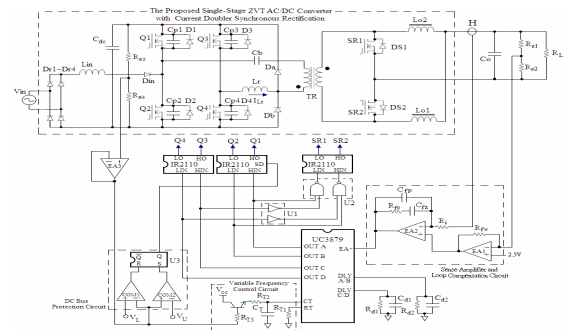$$L_o \geq \frac{2(1-\delta)V_o}{f_{s(min)} \Delta I_{o(pk-pk)}}, \quad (19)$$

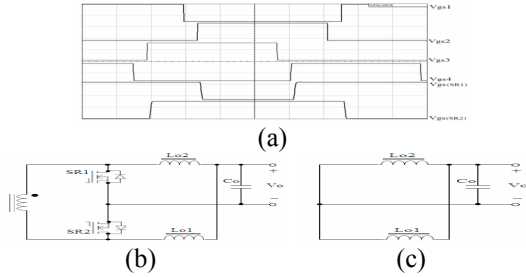Fig. 6 The schematic diagram of the proposed control circuit

(a)

(b)   (c)

Fig. 7(a) The simulation waveforms for verifying the gating logic of the synchronous switches(b) Current doubler synchronous rectification (c) Equivalent circuit in passive intervals

V.   Simulation and Experimental Verification

To verify the feasibility of the proposed single-stage AC/DC converter, a laboratory prototype as shown in Fig. 8 was built to convert a $115V_{rms}$/400Hz source into $5V_{DC}$/100A output for the PAS antenna. The design procedure for the prototype is summarized as follows: Select a nominal duty ratio δ=0.25 and an average DC bus voltage V_{Bus}=400V. Based on Equation (10), the parameter $M_{DC/DC}$ and transformer turn ratio, n can be determined as 0.0125 and 20. From the input voltage specification, the parameter M_{PFC} can be calculated as 2.46. We assumed $\eta_{(DC/DC)}$=90%, the input inductance L_{in} can be selected as 130μH according to Equation (16). The maximum input inductor current, $I_{Lin(max)}$ is determined as approximately 12.5A. Select power MOSFETs IRF460 as the common switch Q2, IRF840 as the other primary switches Q1, Q3 and Q4, then find the parasitic capacitances from the datasheet: C_{p2}=870pF and C_{p1}=C_{p3}=C_{p4}=310pF. From Equation (2), a resonant inductance L_r is selected as 47μH. Typically, the ripple currents on the output inductors are requested at about 25% of the full load current. Therefore, the output inductance can be determined as L_{o1}=L_{o2}=6μH. The circuit parameters of this design example are listed Table 3. Fig. 9 shows the simulation and experimental results to verify the feasibility. Figures 9(a) and (b) show the simulation and experimental waveforms illustrating the ZVS feature. Figures 9(c) and (d) show the simulation and experimental waveforms of the output-side currents I_{Lo1}, I_{Lo2} and I_o'. Ripple cancellation between the two output inductor currents was observed. Figures 9(e) and (f) illustrate the suppression of parasitic ringing by the addition of ring-free diodes. It is clear that the parasitic ringing could be reduced. The snubber circuits, which cause additional power dissipation, are not required. Because of parasitic ringing suppression, the EMI feature of the proposed converter could be improved. Figure 9(g) shows the simulation waveforms of the AC source voltage V_{in} and inductor current I_{Lin}. Figure 9(h) depicts the filtered 400 Hz source voltage V_{in} and current I_{in} waveforms of the laboratory prototype. By adding a small filter capacitor, the proposed converter shows a high power factor and low current harmonics features. Figure 10 shows the measured efficiencies of the proposed AC/DC converter under the output current variation. It is clear that the conversion efficiency can be greatly
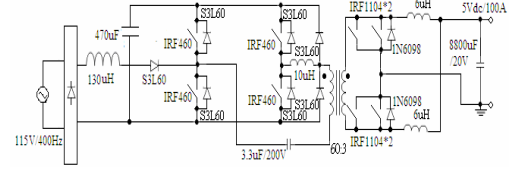
improved.

Fig. 8 The schematic diagram for the laboratory prototype

(a)   (b)

(c)   (d)

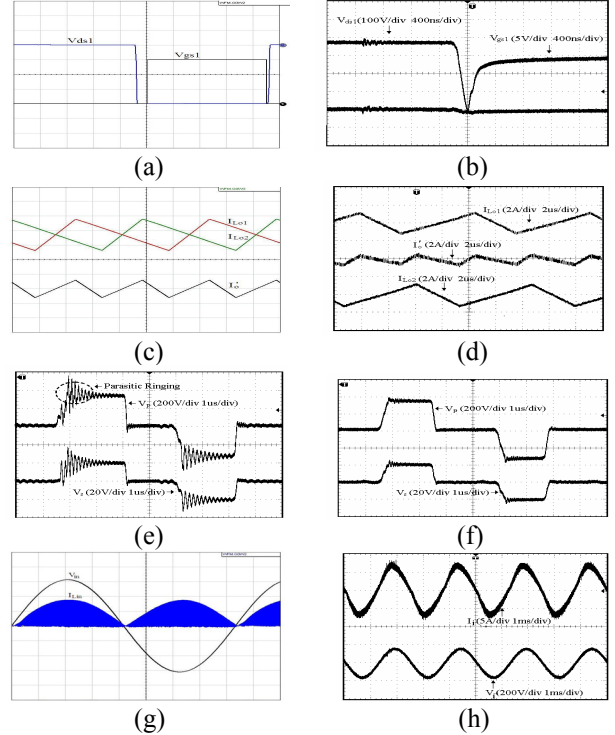(e)   (f)

(g)   (h)

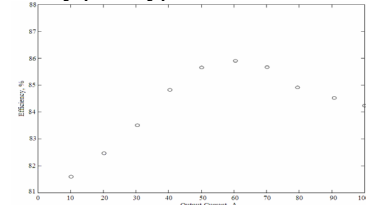Fig. 9 Simulation and experimental waveforms of the laboratory prototype

Fig. 10 The measured efficiencies under the output current variation

Table 1 The current harmonic specifications for a commercial aircraft power system

Harmonics	Current Harmonic Limit
even	1%
3	5%
5	6%
7	4.3%
9	1.67%
11	2.7%
13	2.3%
15	1%
17	1.8%
19	1.6%
21	0.7%
23	1.3%
25	1.2%

<2.5μF per phase per kVA capacitance allowed

Table 2 Switching states of the synchronous switches (SR1 SR2)

Q1 Q2 \ Q3 Q4	0 0	0 1	1 1	1 0
0 0	(x x)	(1 1)	(x x)	(1 1)
0 1	(0 1)	(1 1)	(x x)	(0 1)
1 1	(x x)	(x x)	(x x)	(x x)
1 0	(1 0)	(1 0)	(x x)	(1 1)

Table 3 The circuit parameters of a design example

Parameter	Symbol	Value
Source voltage	V_{in}	$115V_{rms}$
Line frequency	f_i	400Hz
Output voltage	V_o	$5V_{dc}$
Output current	I_o	100A
Input inductor	L_{in}	130μH
Output inductor	L_{o1}, L_{o2}	6μH
External resonant inductor	L_e	17μH
Transformer turn ratio	n	60:3
Transformer leakage inductance	L_l	30μH
DC bus capacitor	C_{dc}	470μF
Output capacitor	C_o	8800μF

VI. Conclusion

In this paper, a high efficiency single-stage AC/DC converter for commercial aircraft power system applications was introduced. The input current harmonics and conversion efficiency could be greatly improved by employing the proposed single-stage topology. The proposed PAS power system has ring-free and low EMI features. Detailed operating principles and design criteria for the proposed converter were described. The IsSpice simulation and performance measurement of a laboratory prototype were performed to verify the feasibility of the proposed method. The results were satisfactory.

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