

An Efficient Correlation Scheme for the GPS Software Receiver

Deok Won Lim*, Deuk Jae Cho*, Chansik park** and Sang Jeong Lee ***

*Department of Electronics Engineering, Chungnam National University, Daejeon, Korea
(Tel : +82-42-825-3991; E-mail: hero0710@cslab.cnu.ac.kr)

**School of Electrical and Computer Engineering, Chungbuk National University, Cheongju, Korea
(Tel : +82-43-261-3259; E-mail: chansp@cbucc.chungbuk.ac.kr)

***Department of Electrical and Computer Engineering, Chungnam National University, Daejeon, Korea
(Tel : +82-42-821-6582; E-mail: eesjl@cslab.cnu.ac.kr)

Abstract: The GPS software receiver based on the SDR(Software Defined Radio) technology provides the ability to easily adopt other signal processing algorithms without changing or modifying the hardware of the GPS receiver. However, it is difficult to implement the GPS software receiver using a commercial processor because of heavy computation load for processing the GPS signals in real time. This paper proposes an efficient GPS signal processing scheme and correlator structure to reduce the computation load for processing the GPS signal in the GPS software receiver, which uses a patterned look-up table method to generate the correlation value between the GPS signals and the replica signals. In this paper, it is explained that the computation load of the proposed scheme is much smaller than that of the previous GPS signal processing scheme. Finally, the processing time of the proposed scheme is compared with that of the previous scheme, and the improvement is shown from the viewpoint of the computation load.

Keywords: Software Receiver, SDR, Correlator

1. INTRODUCTION

Recently, the GPS receiver design using the SDR(Software Defined Radio) technology has been done by many researchers. The SDR technology permits the communication schemes to be modified easily because the digital processing part is implemented by software with minimal RF part. Therefore, it is very interesting subject for the communication systems as well as for GPS receivers[1]-[3]. The GPS software receiver has no need to change the hardware in the case of adopting the advanced algorithms or processing schemes. It has benefits of flexibility and reconstruction, which are weak points of previous hardware implemented GPS receiver. But, the GPS software receiver is hard to implement in real-time because the commercial processor needs to handle large size of data to implement the multiple correlators for the GPS signal[3][4].

To diminish the quantity of operations, an advanced signal processing scheme and the corresponding correlator structure are proposed in this paper. The signal processing scheme can compute the correlation value of 4-samples IF signal at once through the encoded look-up table. And the advanced correlator structure is designed to treat 16-samples IF signal at a time.

Section 2 explains the problems of the typical GPS receiver in a point of the GPS software receiver. Section 3 describes the proposed signal processing scheme and the correlator structure efficient for reducing the computation loads. Section 4 presents some performance results regarding the processing time and the computation loads. Finally, summary and concluding remarks will be given.

2. TYPICAL SIGNAL PROCESSING SCHEMES OF THE GPS RECEIVER

A typical GPS receiver consists of antenna, RF/IF part, digital signal processor and microprocessor (see Fig. 1). Among these, the role of the RF/IF part is to convert the GPS signal into the quantized IF signal. And this signal is

transferred to the digital signal processor after sampling. The main function of the digital signal processor is to wipe off the carrier and code, and give the error signals to tracking loops for synchronization[6][7]. If the carrier and code are locked, the microprocessor will output the navigation data.

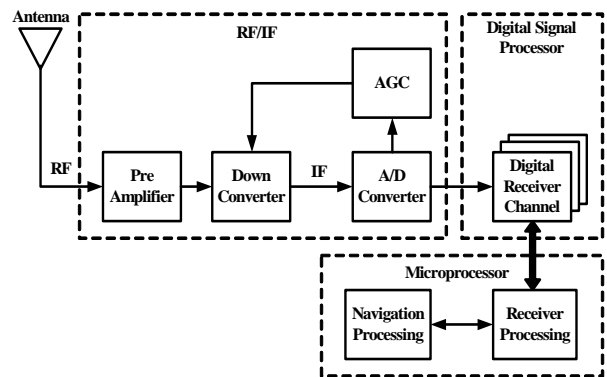


Fig. 1 Typical GPS receivers

In Fig. 2, the typical scheme of digital signal processing is shown.

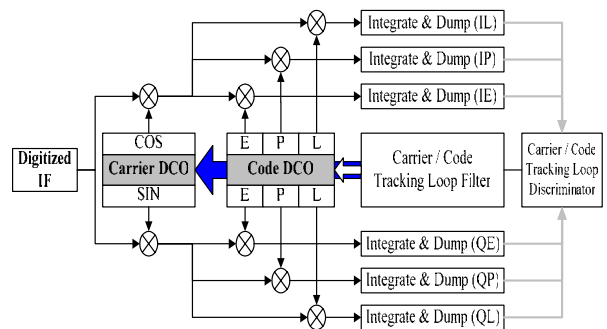


Fig. 2 Typical digital signal processing scheme

The typical digital signal processor mixes the IF signal with the replica signal and accumulates the mixed signals during the period of the C/A code. Using these accumulation values, the digital signal processor synchronizes the IF signal with the replica signal and demodulates the navigation data after synchronization [6].

If the 5.714MHz sampling frequency is used, the accumulator would sum up the 5,714 values for 1-millisecond (see Fig. 3). In other words, the digital signal processor should handle one sample every 175-nanoseconds.

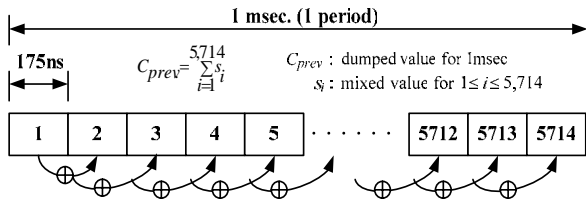


Fig. 3 The concept of the previous signal processing scheme

As a result, the software GPS receiver executes approximately 548,544,000 multiplications and 411,408,000 summations in one second to operate the 12-channel correlators.

3. PROPOSED SIGNAL PROCESSING SCHEME AND CORRELATOR STRUCTURE

An efficient signal processing scheme and a correlator structure are proposed in this paper. And the architecture of the proposed signal processing scheme is shown in Fig. 4.

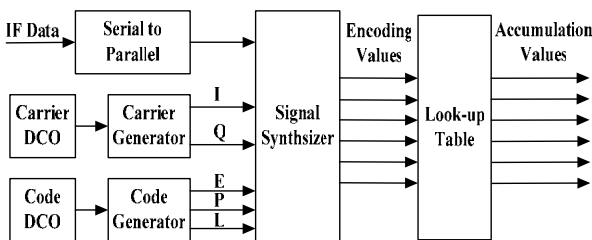


Fig. 4 The block diagram of the proposed signal processing

The Serial to Parallel block converts the 4-samples of 2-bits IF data into the 8-bits parallel data. And the Carrier Generator and Code Generator generate the 4-samples carrier replica and code replica by the Carrier and Code DCO(Digitally Clock Oscillator). Finally, the 4-samples correlation value can be computed by the look-up table at once. Hence, the computation loads are reduced to a quarter as much as that of one sample processing scheme. (see Fig. 5).

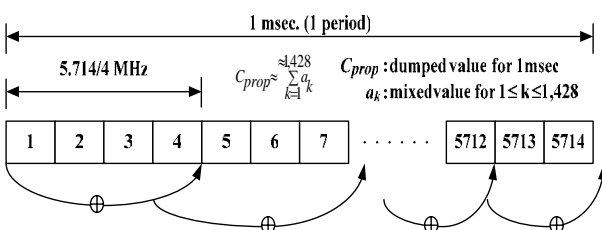


Fig. 5 The concept of the proposed signal processing scheme

In the Carrier Generator, the IN PHASE and QUADRATURE PHASE could be given according to the upper 3-bits of carrier DCO phase as shown in Table 1.

Table 1 The I/Q values according to the DCO phase

DCO Phase [26:24]	IN PHASE	QUADRATURE PHASE
000	1	2
001	2	1
010	2	-1
011	1	-2
100	-1	-2
101	-2	-1
110	-2	1
111	-1	2

In the case of the 5.714MHz sampling frequency, the sampling frequency is about four-times faster than the center frequency of the carrier replica. It means that the carrier replica can be sampled four times in one period. Therefore, if the upper 3-bits of the carrier DCO phase are '001', then it can be estimated that the current value of the IN PHASE is to be '2' and next three values are to be '1, -2, -1' with 92% accuracy[5].

For the above reason, it is able to make the patterns of carrier, and the optimum number of patterns is set to be eight (see Fig. 6).

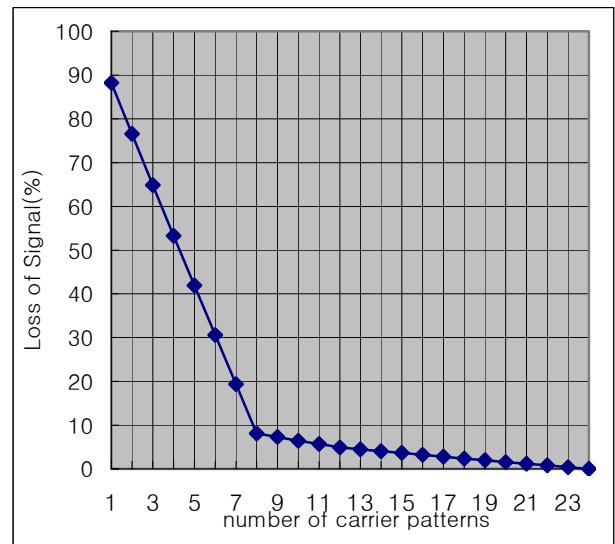


Fig. 6 The probability of the signal loss according to the number of carrier patterns

The 3-bits encoding values according to the carrier pattern are shown in Table 2[5].

Table 2 The carrier patterns and the encoding values

Carrier Pattern				3bits encoding value		
-2	-1	2	1	0	0	0
-2	1	2	-1	0	0	1
-1	-2	1	2	0	1	0
-1	2	1	-2	0	1	1
1	-2	-1	2	1	0	0
1	2	-1	-2	1	0	1
2	-1	-2	1	1	1	0
2	1	-2	-1	1	1	1

The code patterns are shown in Table 3.

Table 3 The code patterns and the encoding values

Code Pattern				3bits encoding value		
-1	-1	-1	-1	0	0	0
-1	-1	-1	1	0	0	1
-1	-1	1	1	0	1	0
-1	1	1	1	0	1	1
1	1	1	1	1	0	0
1	1	1	-1	1	0	1
1	1	-1	-1	1	1	0
1	-1	-1	-1	1	1	1

The number of possible patterns should be eight, because the patterns like '1 -1 1 -1' can not occur.

By using frequent patterns, it is possible to obtain the effect of low-pass filtering. Therefore, the bandwidth of the signal may be decreased, and the processing quantities will be diminished.

The patterns of the IF signal and those encoding values are shown in Table 4. It adapts the same encoding method that uses the sign-bit and magnitude-bit, and it is just extended to 8-bits.

Table 4 The IF signal patterns and the encoding value

IF Signal Pattern				8bit encoding value			
-1	-1	-1	-1	00	00	00	00
-1	-1	-1	-3	00	00	00	01
.
.
.
3	3	3	1	11	11	11	10
3	3	3	3	11	11	11	11

An example of adapting the encoding values to the proposed signal processing scheme is shown in Fig. 7.

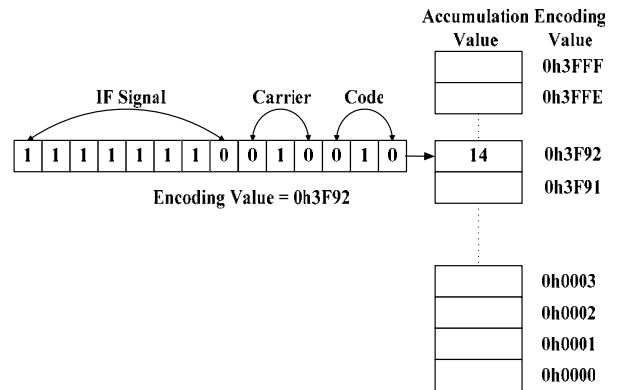


Fig. 7 An example of the proposed signal processing scheme

When the 14-bits encoding value(0h3F92) is made by the encoding values of the IF signal, Carrier and Code replica, the accumulation value(14) is obtained by the look-up table without multiplication.

Table 5 An example of the proposed signal processing scheme

Encoding Bit(14Bits)	11111110 010 010				
IF Data Bit(8Bits)	11111110	3	3	3	1
Carrier Bit(3Bits)	010	-1	-2	1	2
Code Bit(3Bits)	010	-1	-1	1	1
Accumulation Value	3 + 6 + 3 + 2 = 14				

The basic procedure to adapt the proposed signal processing scheme is shown in Fig. 8. It is able to reduce the processing quantities to a quarter as much as that of one sample processing scheme, because it processes the 4-samples at once.

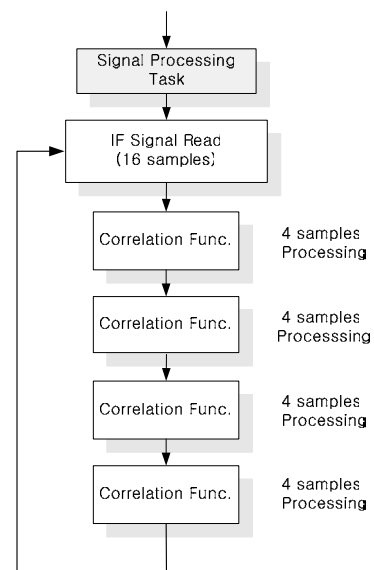


Fig. 8 The procedure of proposed signal processing scheme

Furthermore, it can be improved to process the 16-samples, and the correlation function is advanced as shown in Fig. 9.

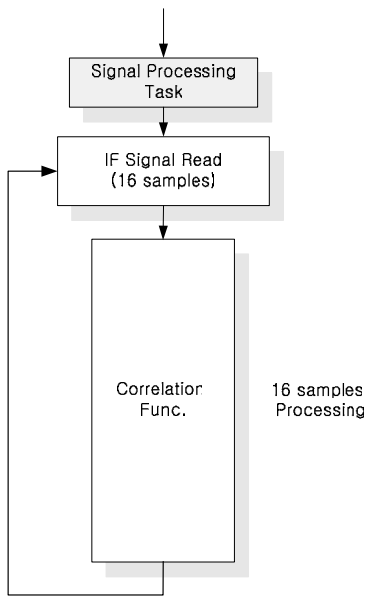


Fig. 9 The proposed procedure

The functional description of the advanced correlation function is shown in Fig. 10.

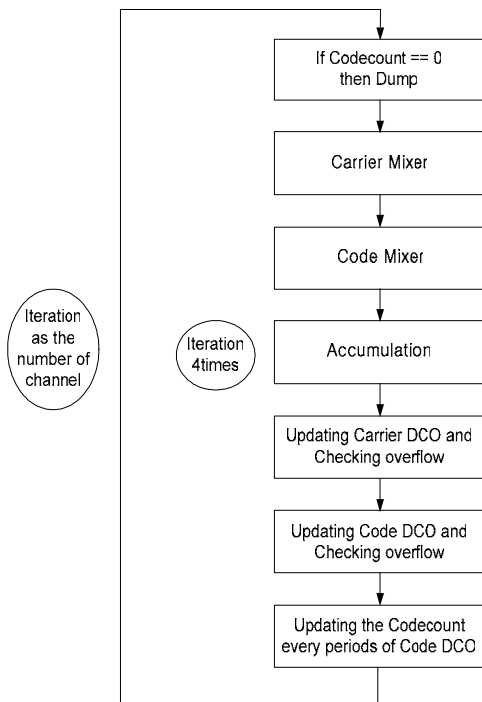


Fig. 10 The functional description of the correlation function

4. PERFORMANCE RESULTS

Prior to presenting the performance regarding processing time, the comparison of the correlation characteristic has been done. The Doppler Effect is not considered herein.

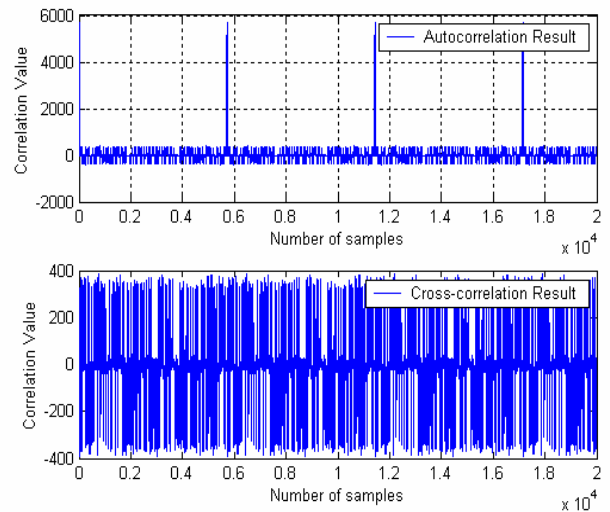


Fig. 11 The correlation results of the previous signal processing scheme

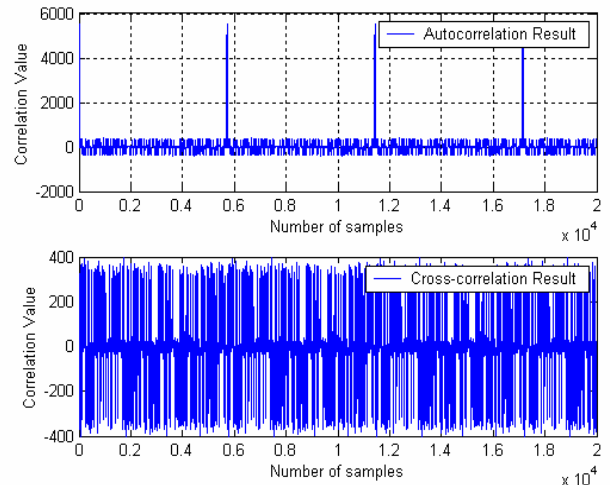


Fig. 12 The correlation results of the proposed signal processing scheme

Table 6 The comparison of the signal processing schemes

	Period	Auto Corr.	Cross Corr.	Ratio
1 sample processing	1msec	5,714	363	23.94 dB
4-sample processing	1msec	5,552	362	23.72 dB

As shown above, the proposed scheme has a 0.22dB correlation loss compared with the one sample processing scheme.

Followings are the results of comparison between the one sample processing scheme and the proposed scheme through the software receiver based on the 2.4GHz PC. The processing time is reduced to a quarter as much as that of the 1-sample processing scheme with the 0.3dB-SNR loss.

Table 7 The comparison of processing time

	IF signal Length	# of channel	Process Time	SNR [dB]
1-sample processing	60 sec.	12	20' 37"	15.0 ~ 15.6
4-sample processing	60 sec.	12	5' 12"	14.8 ~ 15.3

After adapting the proposed scheme and structure, the processing time by inactivating the correlation function is shown in Table 8.

Table 8 The processing time by inactivating the correlation function

# of channel	The processing time with correlation function inactive		
	1-sample processing	4-sample processing	Advanced 4-sample processing
1	176" / 60"	46" / 60"	45" / 60"
2	179" / 60"	47" / 60"	45" / 60"
3	184" / 60"	48" / 60"	45" / 60"
4	195" / 60"	50" / 60"	45" / 60"
8	277" / 60"	70" / 60"	45" / 60"
12	302" / 60"	78" / 60"	45" / 60"

In case of improving the signal processing scheme only, the processing time increases according to the number of channel and exceeds the 60-seconds although the correlation function does not operate. In case of improving the correlator structure, however, the processing time is constant as 45-seconds, which will make real-time processing possible.

After adapting the proposed scheme and structure, the processing time by activating the correlation function is shown in Table 9.

Table 9 The processing time by activating the correlation function

# of channel	The processing time with correlation function active		
	1-sample processing	4-sample processing	Advanced 4-sample processing
1	3' 16"	50" / 60"	45" / 60"
2	5' 29"	84" / 60"	46" / 60"
3	6' 14"	98" / 60"	77" / 60"
4	7' 55"	114" / 60"	82" / 60"
8	13' 49"	216" / 60"	138" / 60"
12	20' 37"	312" / 60"	179" / 60"

In case of improving the signal processing scheme and correlator structure, the processing time has been reduced to 57% of 4-sample processing scheme and 15% of 1-sample processing scheme.

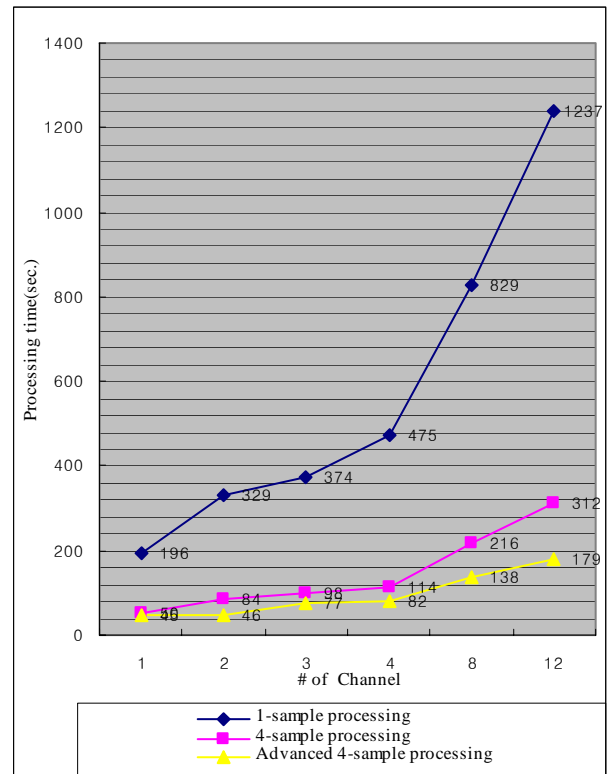


Fig. 13 The comparison of the processing time

Therefore, it can process the 2-channel correlators in real-time and if it should lower the capability of positioning, then it will be able to process about 4~5 channel correlators in real-time.

5. SUMMARY AND CONCLUSION

The efficient signal processing scheme and correlator structure running on a commercial PC have been implemented and tested. The proposed signal processing scheme uses the patterns of high frequency and processes 4-samples IF signal at once. And the correlator structure is modified to adopt the proposed processing scheme efficiently. The processing time is reduced to 15% of 1-sample processing scheme although the 0.3dB SNR loss occurs.

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