Bi-directional Multiple-Input Maximum Circuit in Current-mode

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Abstract: This paper presents the realization of a multiple-input maximum circuit, which is operated in a current-mode. The proposed circuit operates with bi-directional input current signal and employs 5n+4 transistors for n inputs. The realization method is suitable for fabrication using CMOS technology. The proposed circuit is useful building block for the real-time systems. The performances of the proposed bi-directional maximum circuit were studied using the PSPICE analog simulation program. The simulation results verified the circuit performances are agreed with the expected values.

Keywords: maximum operation, current-mode circuit, CMOS-based circuit

1. INTRODUCTION

The analog maximum operation is often required in some real-time applications of analog signal processing such as image processing and fuzzy applications. The realization of maximum function with multiple input in analog circuit form has been implemented using the binary tree structure based on the two-input maximum circuit [1]. The problems of this realization are accumulated errors and low operation speed. To minimize these disadvantages, the one-stage multiple-input maximum circuits have been proposed [2]-[3]. These approaches can be operated only one flow direction of all input currents. When the maximum circuit can be realized with bi-directional operation, the advantage will be gained [4]. The disadvantage of the CMOS-based approach in [4] is the operation mode change of MOS transistors between the saturation and non-saturation regions that causes the distortion on the output signal and limits the operating speed.

The purpose of this paper is to present a bi-directional maximum circuit for multiple input currents, which has the realization method based on the use of a CMOS class AB configuration to improve the circuit performances. The proposed scheme has the simple and modular structure, so it can be easily expanded to meet the requirement of the 5n+4 transistors for n-input maximum circuit. The simulation results supporting the characteristics of the proposed circuit are also included.

2. CIRCUIT DESCRIPTION

From basically design of the proposed circuit, the transistors are all matched and operated in their saturation regions. The drain current of MOS transistor operated in saturation region is expressed as

$$i_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(v_{GS} - V_T)^2 = K(v_{GS} - V_T)^2 \quad (1)$$

where K, v_{GS}, and V_T are the device transconductance parameter, the gate-source voltage, and the threshold voltage, respectively.

2.1 Multiple-input Max scheme

The current-mode multiple-input maximum operation scheme [3] with a very sharp corner in the transfer characteristic is shown in Fig. 1. Each Max cell for one input variable is composed of three transistors, M_{n1}, M_{n2}, and M_{n3}. The transistors M_{n1} and M_{n2} function as the current maximum selector. The transistor M_b and the bias current source I_{B1}, provide the bias voltage V_{B1} approximately equal to $3V_T$. Therefore, the transistors M_{n1}-M_{n3} are forced to the edge of conduction to minimize the crossover distortion. The diode connected transistor M_a and the transistor M_c form of the output signal as the unity-gain positive current mirror to capture the maximum current to output node. The maximum operation of this scheme, based on the shared gate-source voltage corresponding to the saturation value imposed by the maximum input current, can be discussed as follow.

Suppose that there is only one maximum input current among i_1, i_2,…, i_n, and the current i_1 is the largest current, which can be stated as

$$i_1 = \max(i_1, i_2, ..., i_n) \quad (2)$$

The drain-source voltages v_1, v_2,…, v_n of the transistors M_{11}, M_{21},…, M_{n1} established by the input currents i_1, i_2,…, i_n, respectively. The drain-source voltage v_1 is established by the maximum input current i_1, thus the voltage v_1 is the maximum voltage.

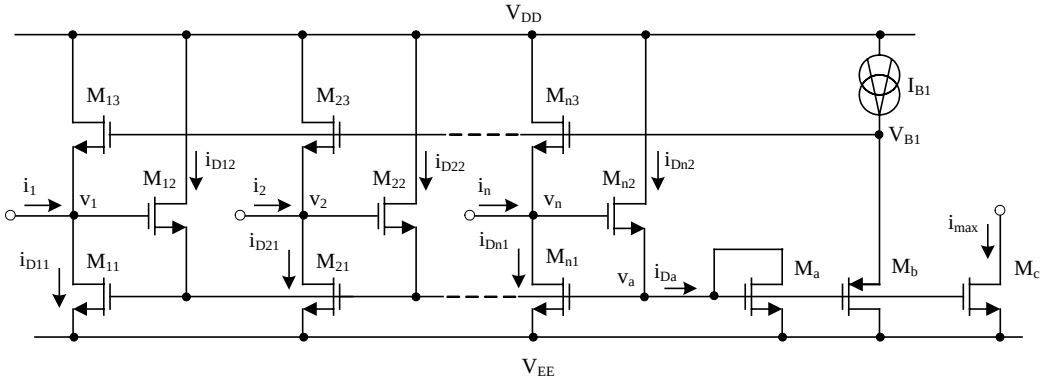


Fig. 1 Multiple-input Max scheme

The gates of transistor M_{11}, M_{21},…, M_{n1}, and M_a are connected together. Then the gate-source voltages can be given by

$$v_{GS11} = v_{GS21} = ... = v_{GSn1} = v_a \quad (3)$$

Based on Eqs. (1)~(3), the transistors M_{11}, M_{21},…, M_{n1}, and M_a have the same drain current as

$$i_{D11} = i_{D11} = ... = i_{Dn1} = i_{Da} = i_1 \quad (4)$$

In saturation, the current i_{D21} flows through the transistor M_{21} increasing the gate-source voltage of the transistor M_{21}, which effects the transistor M_{22} to cutoff. Similarly, The flow of i_{D31}, i_{D41},…, i_{Dn1} through the transistor M_{31}, M_{41},…, M_{n1} causes the transistor M_{32}, M_{42}, …, M_{n2} to cutoff. Therefore the drain currents i_{D22}, i_{D32},…, and i_{Dn2} can be given by

$$i_{D22} = i_{D32} = ... = i_{Dn2} = 0 \quad (5)$$

Considering at node v_a, the drain current i_{Da} can be expressed as

$$i_{Da} = i_{D12} + i_{D22} + ... + i_{Dn2} \quad (6)$$

Substituting Eq. (5) into Eq. (6), we obtain

$$i_{Da} = i_{D12} = i_1 \quad (7)$$

The current i_{Da} is mirrored into output node by the current mirror M_a and M_c. Then the maximum output current i_{max} can be given by

$$i_{max} = i_1 = \max(i_1, i_2, ..., i_n) \quad (8)$$

The above discussion supports the maximum operation of the multiple current signals.

From the circuit in Fig. 1 the input current is restricted by one-direction current. If the max-circuit can operate with bi-direction input current then the advantage will be gained.

2.2 The proposed Bi-direction maximum circuit

Fig. 2 shows the proposed bi-direction maximum circuit for the multiple-input currents, which based on the use of the multiple-input Max scheme in Fig. 1. For one input signal, the cell consists of five transistors, M_{n1}-M_{n5}. The transistors M_{n4}-M_{n5}, M_d and the current source I_{B2} function as the minimum cell [5], where M_{n4} acts as a current limiter, M_{n5} from the multiple input source-coupled circuit, and I_{B2} is used to bias the multiple input source-coupled circuit. The transistor M_d is used to capture the minimum current to node A.

The proposed bi-direction maximum circuit operation is as follows. At first, consider that all input currents are positive currents $i_n > 0$, and suppose that the current i_1 is the maximum input current among i_1, i_2, …, i_n. From the maximum operation of the proposed circuit can be discussed as section 2.1, the drain-source voltage v_1 is established by the maximum input current i_1, thus the voltage v_1 is the maximum voltage. The matched NMOS transistors M_{11}, M_{21}, …, M_{n1} and M_a have the same gate-source voltage v_1, so, in saturation, they should also have the same drain current as

$$i_{D11} = i_{D21} = ... = i_{Dn1} = i_{Da} = i_{Dc} = i_1 \quad (9)$$

Considering at each input node v_n, the input current i_n can be written as

$$i_n = i_{Dn1} - i_{Dn4} \quad (10)$$

Based on the Eq. (9) and Eq. (10), the drain current i_{Dn4} of transistor M_{n4} can be given by

$$i_{D14} = 0, i_{D24} = i_1 - i_2, i_{D34} = i_1 - i_3, ..., i_{Dn4} = i_1 - i_n \quad (11)$$

Based on the Eq. (11), the voltage v'_1 established by the minimum drain current i_{D14} will be the maximum voltage among v_1, v_2, …, v_n. From the voltage v'_1 is maximum voltage effecting the other transistors M_{25}, …, M_{n5} to cutoff, Then the current I_{B2} will flow through the transistor M_{15}. Such as, the common voltage V_{cm} connected to the gates of transistors M_{n4}s will follow the voltage v'_1 generated by the minimum current i_{D14} among the drain currents i_{D14}, i_{D24},…, i_{Dn4}. Since the source-gate voltages of transistors M_{n4} are equal to V_{DD}-V_{cm}, the increasing in V_{cm} will result in the decreasing of the current flowing through these transistors. As for the other cells not carrying the minimum input current. Therefore, the drain current i_{Dd} can be given by

$$i_{Dd} = \min(i_{D14}, i_{D24}, ..., i_{Dn4}) = i_{D14} = 0 \quad (12)$$

At node A, the drain current i_{out} can be written as

$$i_{out} = i_{Dc} - i_{Dd} = i_1 - 0 = i_1 \quad (13)$$

On the other hand, consider another case when all input currents are negative currents $i_n < 0$ and suppose that the current i_2 is the maximum input current among i_1, i_2, …, i_n. From the maximum operation of the proposed circuit discussed in section 2.1, the transistors M_{11}, M_{22}, …, M_{n2} of the maximum circuit are cutoff. So, the drain current of transistors M_{11}, M_{21}, …, M_{n1}, M_a and M_c can be given by

$$i_{D11} = i_{D21} = ... = i_{Dn1} = i_{Da} = i_{Dc} = 0 \quad (14)$$

Considering at the minimum cell, the drain current i_{Dn4} of transistor M_{n4} can be given by

$$i_{D14} = 0 - i_1, i_{D24} = 0 - i_2, ..., i_{Dn4} = 0 - i_n \quad (15)$$

or

$$i_{D14} = -i_1, i_{D24} = -i_2, ..., i_{Dn4} = -i_n \quad (16)$$

Then the output current of minimum cell i_{Dd} can be given by

$$i_{Dd} = \min(i_{D14}, i_{D24}, ..., i_{Dn4}) = i_{D24} = -i_2 \quad (17)$$

At node A, the drain current i_{out} can be written as

$$i_{out} = i_{Dc} - i_{Dd} = 0 - (-i_2) = i_2 \quad (18)$$

It is clearly seen that the proposed maximum circuit for the multiple-input currents can operate with bi-direction input current and the number of transistors for an n-input bi-directional maximum circuit is 5n+4.

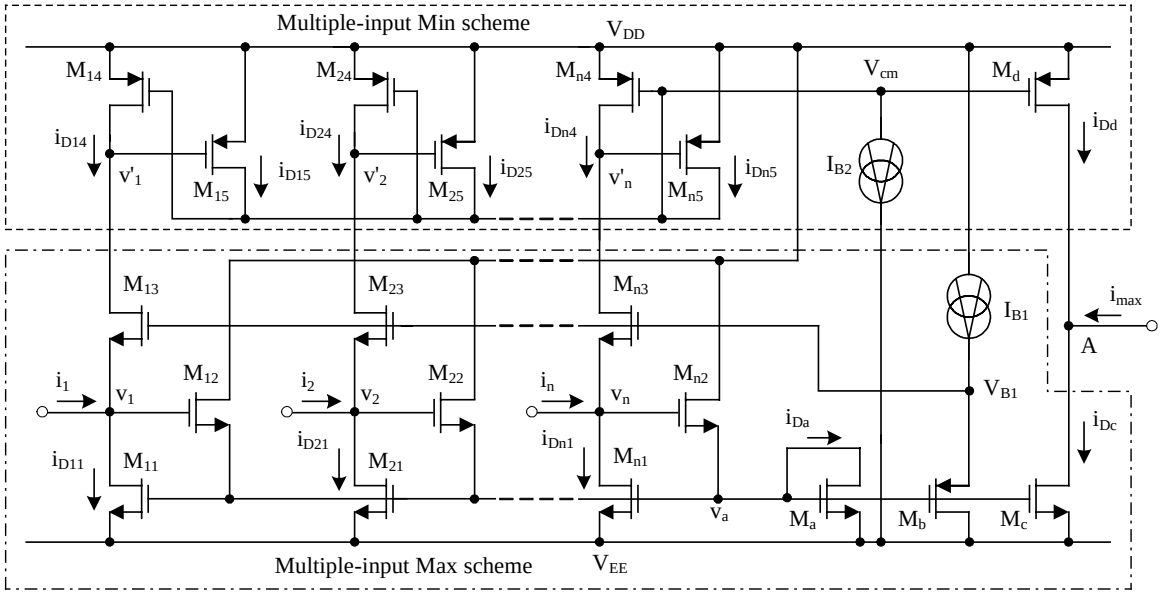


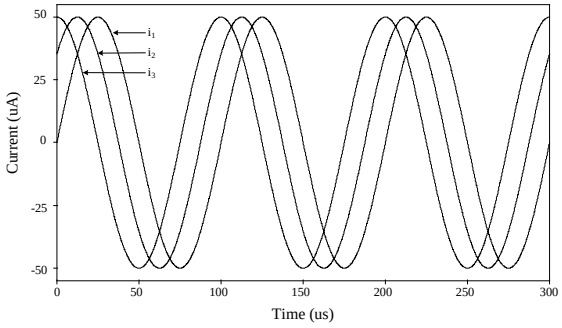
Fig. 2 Proposed bi-directional multiple-input maximum circuit

3. SIMULATION RESULTS

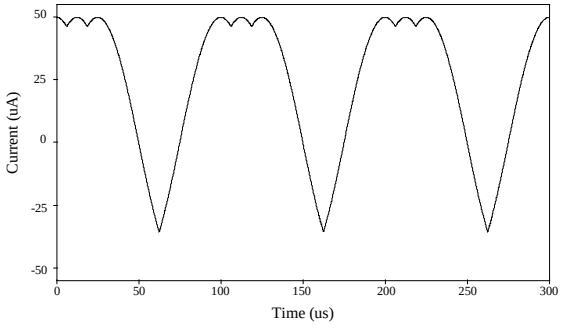
To verify the performances of the proposed bi-directional maximum circuit in Fig. 2 has been simulated with the PSPICE analog simulation program. The BSIM MOS model of the 0.5μm CMOS process was used for the circuit simulation. The proposed circuit simulations, the dimensions W/L of the devices used are shown in Table 1. The bias current source I_{B1} and I_{B2} are set to 20μA and 0.5μA, respectively. The supply voltages are taken as V_{DD}=+3V and V_{SS}=-3V. Fig. 3 shows the transient-response of the proposed three-input circuit. Where the input currents i_1, i_2, and i_3 are 10kHz sinusoidal wave with 50μA peak amplitude, and 0°, 45°, and 90° phase shift, respectively. Fig. 4 shows the transient-response of the proposed three-input circuit. Where the input currents i_1 is the triangular input current with 50μA peak amplitude and 100μs time period, and the input current i_2 and i_3 is the constant current, which set to -25μA. Fig. 5 shows the frequency response of the proposed circuit. It should be noted that a bandwidth of approximately 78MHz is observed. It is evident that the performance of the proposed circuit exhibits a high accuracy and high-speed operation.

Table 1: Dimensions of the CMOS transistors

Transistors	W(μm)/L(μm)
M_{n1}, M_a, M_b, M_c	4/1
M_{n2}	8/1
M_{n3}	2/1
M_{n4},M_d	4/2
M_{n5}	8/2

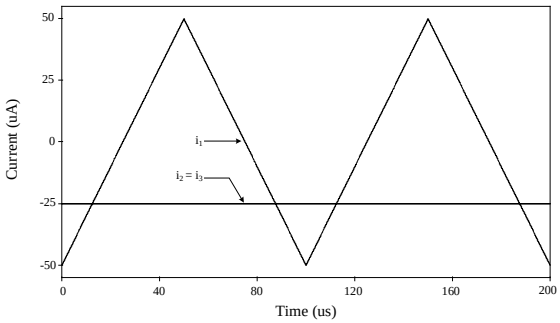


(a)

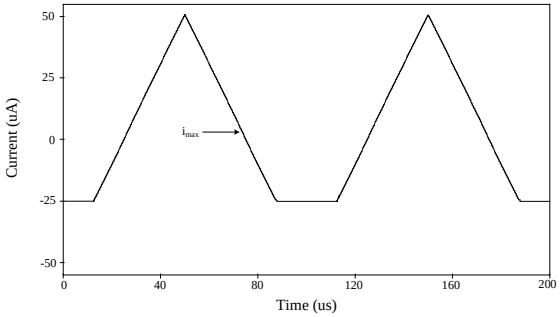


(b)

Fig. 3 Transient-response of the proposed three-input circuit
(a) Sinusoidal three input currents
(b) the maximum output current



(a)



(b)

Fig. 4 Transient-response of the proposed three-input circuit
(a) the input current
(b) the maximum output current

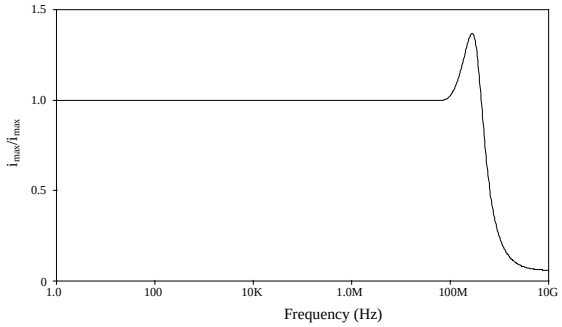


Fig. 5 Frequency response

4. CONCLUSION

In this paper, a multiple-input maximum circuit for the bi-directional input current has been presented. The proposed circuit designed with 5n+4 transistors, where n is the number of input current signals. This structure is simple and modular, so it can be easily expanded to meet the requirement of the number of multiple-input signals. From the simulation results, it is evident that the proposed bi-directional multiple-input maximum circuit functions correctly and provides excellent performances.

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