Design of Programmable Logic Controller and I/O Expansions

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Abstract. This paper presents a design of Programmable logic Controllers which are well known for a long time that can be applied to be a controller for an automatic machine in industries. However, most of them have been imported from oversea country. This research focuses on the development of PLC by KMITL staff. This PLC system is consists of CPU unit, Digital I/O RTU unit, ANALOG RTU unit. The implementation of the CPU scan time and I/O refresh are principle to PLC. In this article, there are many benefits to industries especially in order to support SME that can use local technology. Therefore, we can apply this research to the manufacturing process in Thailand for the future.

Keywords: PLC, RTU, Scan time

1. INTRODUCTION

Programmable Logic Controller in Thailand has been applied commonly around year 1985 King Mongkut's Institute of Technology, Chaokhuntaharn Ladkrabang (KMITL), Instrumentation Engineering Department get some supports from UNDP. (UNITED NATIONS DEVELOPMENT PROGRAM) for 2 years in sponsoring Thai lecturers aboard to learn technology in Europe and sending consultants to the institute. During the beginning period, PLC laboratory is one the laboratory that get funding from UNDP. in this project. Most equipments, especially PLC, were imported. The department realized this importance, so this research was initiated. The development has been continued, sometimes has some difficulty the causes delayed project. However, the attempt make this project success in 1990, from that period, there are some improvements, tests continuously until now. The development will focus on the research that can serve local needs for small industries and study test kits. So the HARD WARE will be designed to served industries objectives

This research will describe that designed PLC structure consists of base units, remote terminal units, memory maps, instruction command and Operating System as well as system testing

2. PLC STRUCTURE

PLC structure consists of parts that can be put in diagram in fig.1

1. Central processing units (CPU)
2. Input/output units
3. Remote terminal units (RTU)

2.1 Central Processing Unit

Central Processing Unit or base unit is designed by microprocessor. It's function is to control process by receiving input status from device, computing program according to written program and sending the computed result to output device that operated by Operating System. Input will get status from push button switch, sensor from machine. For the PLC command, there are many command groups e.g. logic, movement, arithmetic, timer/counter commands etc this research report is designed by microprocessor 8 bits/ 16 bits series Z84C11 which is 100 pin CPU, the input/output ports can be connected to external devices 4 ports and serial communication 2 ports, speed of crystal 10 MHz. 32 Kbytes ROM is an operating system (OS). 32 Kbytes RAM is user program and executed memory. All of systems are designed to meet local industry objectives. There are various sizes of IO matched with machines, so it's economical in order to support small and medium industries.

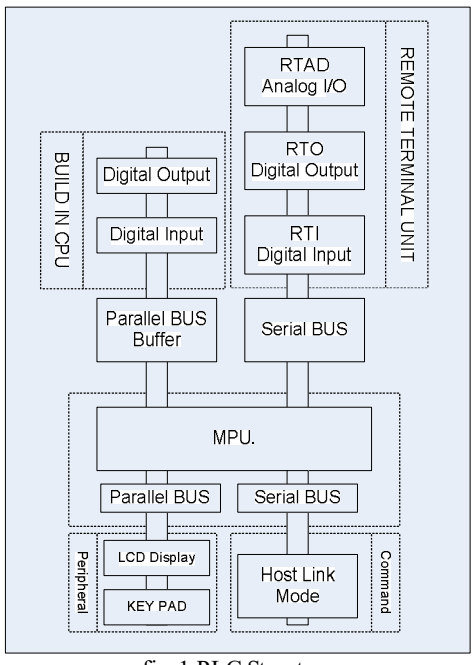


fig. 1 PLC Structure

2.2 Input/output Units

Input/output units are built in Base Unit, Input terminal is connected to input devices in fig.2, e.g. proximity switch are used for non-contact object detection. They integrate a sensing element and a transistor NPN switch output which connected to DC. Voltage Digital sink input circuit of PLC.(1)

Output terminal is connected to output devices in fig.3, it shows a typical opto-isolated NPN transistor switch output circuit.

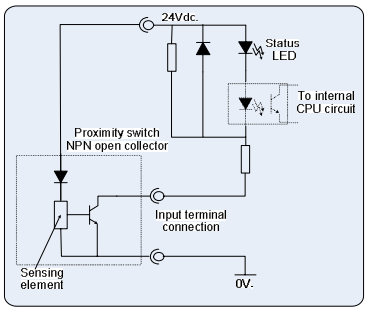


Fig.2 DC. Voltage Digital sink input circuit

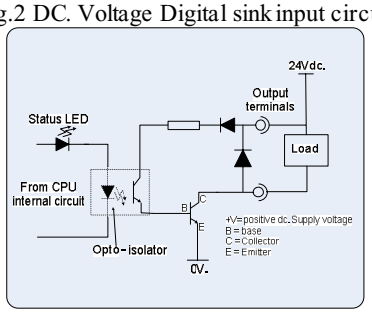


Fig.3 DC. Voltage Digital NPN transistor output circuit

2.3 Remote terminal Units (RTU)

Remote terminal units are distributed through network device group, centralized by PLC control and communicated with similar protocol through serial bus in IEC fieldbus RS485 standards. These networks, often referred to as "data highways", utilize twisted shielded-pair to carry high speed. Communications data between the various Controller and RTUs microprocessor - based devices connected to the network. The RTU network devices consisted of three models, Remote terminal Input 16 (RTI16), Remote terminal output 16 (RTO16) and Remote terminal AD/DA (RTAD). The number of RTUs that can connected to data highway network varies with the network design. The maximum of modules are able to expand to 32 units. RTU designed by microcontroller MSC51 is CPU that operated with Crystal frequency 11.0592 MHz. RAM size 4 Kbytes, ROM size 256 bytes. Max 192 A/D chip support 10 bits 8 channel and 2 Chips 0800 D/A 8bits 1 channel depict fig.4

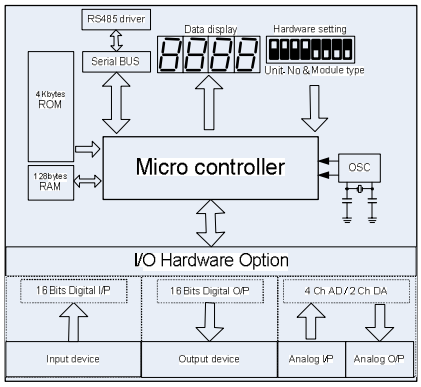


fig.4 :block diagram of RTU units

3. PLC MEMORY ARCHITECTURE(2)

All PLCs contain both RAM and ROM in varying amounts depending upon the design of the PLC. The use of PLC's memory is determined again by the design of the unit. However, all PLC memories can be subdivided into at least five major areas. A typical memory utilization map for a PLC is depicted in table 1.

Table1 CPU memory

Memory	Address Range(Hex)	Size
Executive Memory	0000-7FFFh	32 K
User Memory	8000-9C00h	7K
System Memory	9C01-F100h	21K
Data Memory	F101-FF00h	3.9K
I/O Status Memory		
Stack Memory	FF01-FFFFh	256byte

3.1 Operating system

Operating system or executive memory for the PLC is always placed in ROM since, once developed, it rarely needs changing. The executive of a PLC performs several functions. It is the one that actually does the "Scanning" in a PLC. The PLC user programs the PLC in high-level language composed of relay symbols. These symbols are stored in the user portion of the memory in binary format. The executive causes the microprocessor to examine each user instruction, then instructs the microprocessor through the actual conversion of the high-level instruction into it's equivalent series of machine language instruction for further action by the microprocessor. Often a user program will contain instructions that require data from other areas of the memory. In this case the executive programming must instruct the microprocessor to gather these data along with the proper machine language for further use by the microprocessor

3.2 I/O memory

It's the memory that can be referred to I/O statuses in order to connect with I/O devices. Whenever the executive program instructs the microprocessor to read the current statuses of the inputs to the PLC, it stores this information in the input status or image area. As the executive instructs the microprocessor to scan the user program and interpret the user commands, various output device statuses are generated. These output states and conditions are stored by the microprocessor in the output status or image area until the end of the logic scan when the output modules get updated to this previously stored information. These status areas of memory are always available for user monitoring and use

3.3 System memory

This memory is reserved for program data manipulation. When timers, counters, math, and/or data functions are available, an area of memory must be set aside for data storage. The data storage portion of memory is allocated for storage of such items as timer or counter preset and accumulated values, math instruction data and results, and miscellaneous data and information which will be sued by any data manipulation functions programmed in the user memory area It's placed in RAM.

3.4 User memory.

This memory is allocated to the storage of the user program. It is the memory area that the executive program instructs the microprocessor to examine or "scan" to find the user instructions. The user program are may be subdivided if the processor allocates a portion of this memory area for the storage of ASCII messages, subroutine programs, or other special programming functions or routines. It's placed in RAM

3.5 Stack memory

This memory is served for storage of stack pointer index in order to execute in subroutine program. It's placed in RAM.

Table2 PLC visual memory

Area	Size	Range(word)
Digital Input	32 bits	000-001
Digital Output	16 bits	007
Remote Digital Input	16 bits	00-15
Remote Digital Output	16 bits	00-15
Remote Analog Input/Output	4Ch.ADC 2Ch.DAC	00-15
Internal Relay	1,120 bits	008-0078
Holding Relay	1,600 bits	HR00-HR99
Link Relay	1,024 bits	LR00-LR63
Timer	512 Points	T000-T511
Counter	512 Points	C000-C511

Table2 is classified and adapted from table 1 by OS. developer. Objectives of this re-classification is easy to use. The memory in table 2 is called "Visual Memory"

4. COMMAND AND INTERPRETER

These are important parts of operating systems. They cause the microprocessor to examine each user instruction, then instructs the microprocessor through the actual conversion of the high-level instruction into it's equivalent series of machine language instruction for further action by the microprocessor. User instruction in PLC designs memory units to "RECORD". There are 2 fields in the record, the first one is 'code number' (instruction code), the second one is 'statement' as following table 3

Record format

Record of code command
Code Number :1 Byte;
Statement : 4 Byte;
End.

Table 3 interpreter record

Record No.	Code No.	Statement
0001	Code1	Statement A
0002	Code2	Statement B
0003	Code3	Statement C
End record	Code…	Statement..

There are some samples of Logic, Movement ,Arithmetic Shift , BCD Calculation and Remote I/O instruction code assignments, refer to table 4 to 8 respectively

Table4 Sample of Logic instruction code assignment

Code No.	Statement	Code No.	Statement
80	LD	81	LD NOT
82	LD HR	83	LD NOT HR
84	LD LR	85	LD NOT LR
86	AND	87	AND NOT
88	AND HR	89	AND NOT HR
8A	AND LR	8B	AND NOT LR

Table5 Movement instruction code assignment

CodeNo.	Statement1	Statement2	Statement3	Statement4
A0	MOV(21)	Source	Destination	--
A1	MVN(22)	Source	Destination	--
A2	MOVD(83)	Source	Designation	Destination

Table6 Arithmetic Shift instruction code assignment

CodeNo.	Statement1	Statement2	Statement3	Statement4
B0	ASL(25)	Word	--	--
B1	ASR(26)	Word	--	--
B2	ROL(27)	Word	--	--
B3	ROR(28)	Word	--	--

Table7 BCD Calculation instruction code assignment

CodeNo.	Statement1	Statement2	Statement3	Statement4
C0	ADD(30)	Source	Add	Result
C1	SUB(31)	Source	Su	Result
C2	MUL(32)	Source	Mu	Result
C3	DIV(33)	Source	Dv	Result

Table8 Remote I/O instruction code assignment

CodeNo.	Statement1	Statement2	Statement3	Statement4
D0	RDI(70)	#Unit No.	Source	--
D1	WRO(71)	#Unit No.	Destination	--

Example of programs in operating system that write for microprocessor to operate according to Subroutine LD, LD NOT, OUT and OUT NOT are followings

Instruction routine procedure

Procedure LD command

```
Subroutine LD_SUB;
Begin
  Result:=Datatable (IOassign);
          IF Result>0 then
  Result:=$FF else
          Result:=$00;
          Push result to stack;
 End;
```

Procedure LD NOT command

```
Subroutine LD NOT_SUB;
Begin
          LD_SUB(IOassign);
          Pop result from stack;
          Complement result;
          Push result to stack;
End
```

Procedure OUT command

```
Subroutine OUT_SUB;
Begin
          Pop result from stack;
          Data table(IOassign) :=
Result;
          Push result to stack;
End;
```

Procedure OUT NOT command

```
Subroutine OUT NOT_SUB;
Begin
          Pop result from stack;
          Data table(IOassign) :=
Result;
          Complement result;
          Push result to stack;
End;
```

5. HARDWARE CONFIGULATION

Hardware configuration are consisted of CPU Unit(84PROsf) ,RTU1(RTI16) 16 bits digital input / station #00 and RTU2(RTO16) 16 bits digital output /station #01 as depicted in fig. 5

In one scan time of PLC, starting from reading input status from RTI16, manipulate data or condition according to user program, then update output data to RTO16, the end of scan time depicted in fig. 6

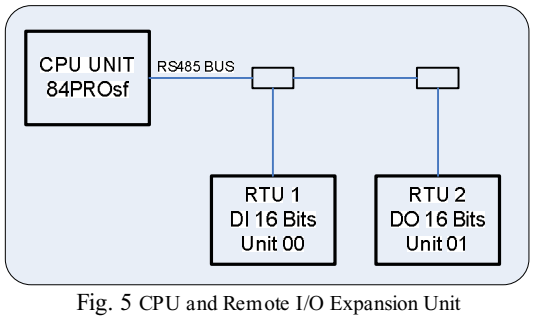


Fig. 5 CPU and Remote I/O Expansion Unit

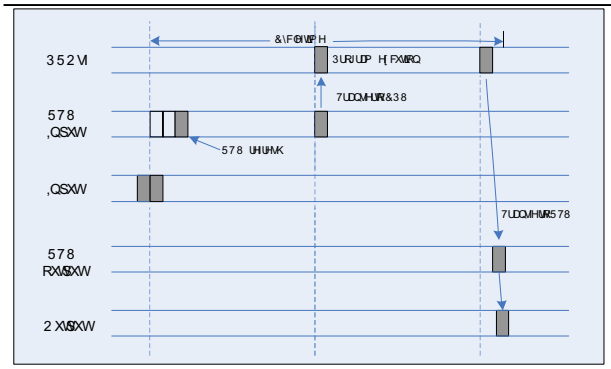


Fig. 6 I/O Respond time diagram

The overall flow of PLC operation is as shown in the following flowchart depicted in fig. 7 [3]

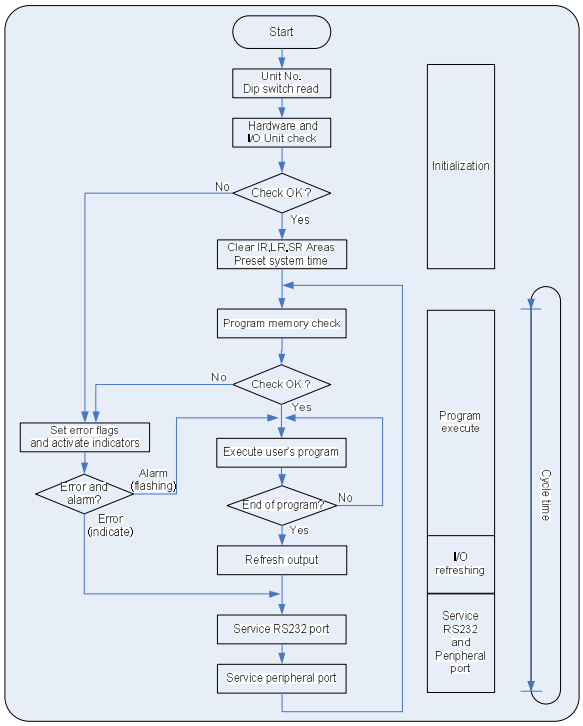


Fig. 7 Operation flow chart in one scan time of PLC

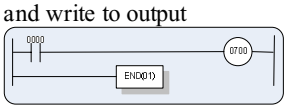
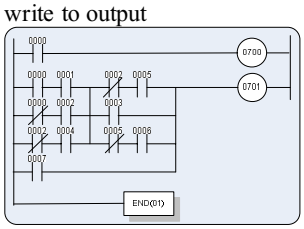
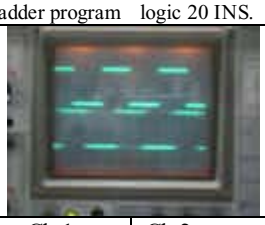
6. IMPLEMENTATION

Response to system in term of PLC scan time is very important. The PLC that have fast scan time can response to the system effectively. This test can measure scan time by using oscilloscope. Testing procedure can be done by pulse signal input at PLC from pulse generator. Range of pulse generator is 1to10 KHz in order to be input signal simulator, then ladder programming to operate test program and write data to output. The oscilloscope has 2 channels, channel 1 and 2, measuring signal from input and output of PLC respectively, as depicted in fig.8

Fig.8 scan time measuring by oscilloscope

Testing procedures consisted of 3 tests as followings

Case test 1,2

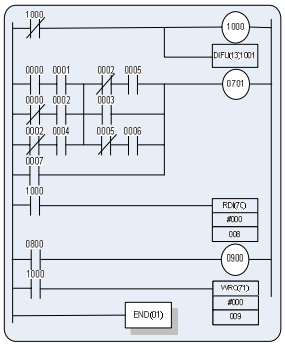
<table>
<tr><td colspan="4">One CPU Unit</td></tr>
<tr><td colspan="2">Read input then compute and write to output
 
Program1
Ladder program I/P and O/P</td><td colspan="2">Read input then compute and write to output
 
Program2
Ladder program logic 20 INS.</td></tr>
<tr><td colspan="2">  </td><td colspan="2">  </td></tr>
<tr><td>Ch.1
Input signal</td><td>Ch.2
output signal delay time</td><td>Ch.1
Input signal</td><td>Ch.2
output signal delay time</td></tr>
<tr><td>4 msec.</td><td>? msec.</td><td>4 msec.</td><td>? msec.</td></tr>
</table>

These tests are used for measuring scanned time of CPU Unit, the processes are as followings

1. Input signal from pulse generator to PLC input address 0000
2. Probe for measuring input signal address 0000 and output signal address 0700 of PLC by Oscilloscope (OSC) in channel 1 and 2 respectively
3. Write the ladder program1 to PLC and selected switch to run mode.

From result of case test 1, The PLC is able to respond pulsed input signal 250 Hz or 4 mSec. and output signal delay time is 0.25 mSec. In case test 2, The processes are similar to case test1 but rewrite the ladder program2 to PLC. In ladder program2, there are 20 logic instructions. The PLC is able to respond pulsed signal input 250 Hz or 4 mSec. and output signal delay time is 0.5 mSec. When compare output delay times of these two tests, the output delay time of case test 1 is shorter than case test2's 0.25 mSec. in execution of 20 instructions.

Case Test 3

<table>
<tr><td colspan="3">CPU +RTI16+RTO16 Unit</td></tr>
<tr><td rowspan="2"> 
Program3
Ladder program and
RDI&WRO command</td><td colspan="2">  </td></tr>
<tr><td>Ch.1
Input signal</td><td>Ch.2
output signal
delay time</td></tr>
<tr><td></td><td>100msec.</td><td>10 msec.</td></tr>
</table>

This test consists of CPU Unit , RTI16 and RTO16, measures scanned time. The processes are as followings

1. Input signal from pulse generator to RTI16 address 0800,
2. Probe for measuring input signal RTI16 address 0800 and output signal RTO16 address 0900 by Oscilloscope(OSC) in channel 1 and 2 respectively
3. Write the ladder program3 to PLC and selected switch to run mode.

From result of case test 3, The PLC is able to respond pulsed input signal 10 Hz or 100 mSec. and output signal delay time is 10 mSec. So the input respond time is relatively long since most time spending to communicate data.

CONCLUSION

Even result of PLC research can response to scanned time speed not as fast as imported PLC, it's meet the department's objective that to depend on our own local technology in order to serve local need in small and medium industries. In testing, the department cooperates with private organization to research and testing by installing with various machines e.g. Screen painting machine of plastic can filling color and oil, small paper cutting machine, KFC. sauce pack filling machine, Reverse Osmosis water production rate 5,000 lits/day for ice industry etc. The testing result is good at one level and will be developed to higher efficacy and better capacity in the future

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