The Analysis of Input Power Matching for CMOS RF Low Noise Amplifier Design

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Abstract

In this paper, the analysis of input power matching for CMOS RF Low Noise Amplifier (LNA) design is introduced. With two input power matching techniques, the performance of LNAs is estimated according to gain and noise figure. This process can be expressed easily by theoretical method and using simulation. These analytical methods are useful in that they can provide enough insights for designing CMOS RF LNAs.

I. Introduction

Continuous advances in a CMOS technology have reduced the minimum gate length of MOS device, improving the microwave performances accordingly. The CMOS technology became a competitive technology for wireless application because it provides such advantages as low cost, high-level integration and easy access over other technologies. In a receiver system, the LNA is the first integrated block. It must achieve signal amplification with a minimum signal-to-noise ration degradation, and also be matched to the 50 Ω impedance standard elements such as bandpass filters of LNA output and antennas of LNA input.

The LNA design involves many tradeoffs between gain, noise figure, power dissipation, etc. In spite of these tradeoffs, the LNA should not only supply high gain but also have low noise figure at any given amount of power dissipation. In this paper, the two LNA designs with different input topology are analyzed based on gain and noise. In Section II, the two input topologies of LNA are analyzed by theological method and then verified by circuit simulation in Section III. Section IV concludes this paper.

II. The two input topologies of LNA

Case A : General input topology

In general, LNA has the commonly used cascode configuration with source degeneration inductor as shown in Fig. 1. Here, the cascode transistor M_2 is used to achieve good

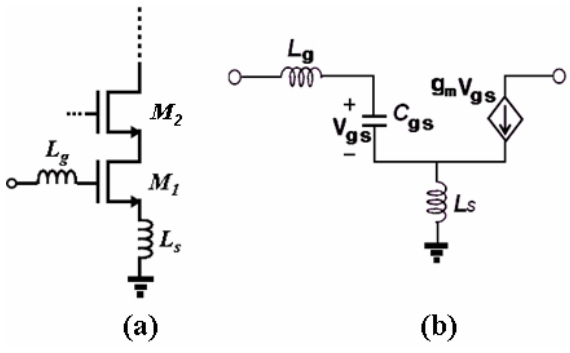

Figure 1. (a) The LNA of Case A structure
(b) Equivalent circuit

reverse isolation. This topology can provide good input, output reflection and simultaneous matching of noise and input in narrow band application. The input impedance of this topology is given below.

$$Z_{in1} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}} L_s \cong s(L_g + L_s) + \frac{1}{sC_{gs}} + f_T L_s \quad (1)$$

To get a 50 Ω input impedance, as we know, the real part of (1) should equal to 50 Ω while the imaginary part should be zero at the frequency of interest. But, as channel length of the

MOSFET is scaling down, f_T is so high that it is hard to get a 50 Ω input impedance due to demanding small inductance of source degeneration inductor. In other words, the smallest inductance of inductor provided by Foundry Companies has larger inductance than we need for 50 Ω input power matching to this case (1). Therefore, because input impedance of the circuit is larger 50 Ω impedance, for 50 Ω input power matching, source degeneration inductor is designed by 3D simulator like HFSS simulator.

The G_m, that is transconductance of this topology, is given below.

$$G_{m1} = \frac{i_D}{v_{in}} = \frac{g_m}{wC_{gs}R_{in}} = Q_{in1} \cdot g_m \qquad (2)$$

Where g_m is transconductance of the MOSFET, R_{in} is the input impedance of 50 Ω and Q_{in1} is the quality factor of the input network of this topology. R_{in} and Q_{in1} are defined below, respectively.

$$R_{in} = \frac{g_m}{C_{gs}} \cdot L_s = 50\Omega \qquad (3)$$

$$Q_{in1} = \frac{1}{wC_{gs}R_{in}} \qquad (4)$$

Case B : General input topology with shunt capacitor

Fig. 2. shows a general cascode topology with shunt capacitor between the gate of the MOSFET M_1 and the ground. The difference in Fig. 2 compared to the Fig. 1 is one additional shunting capacitor C_F.

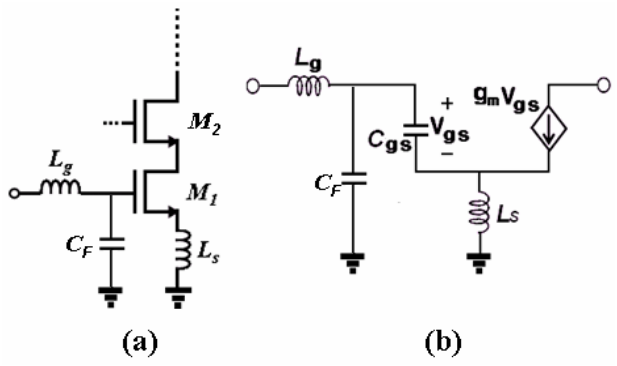

Figure 2. (a) The LNA of Case C structure
(b) Equivalent circuit

As mentioned before, even when we use the smallest inductor for source degeneration among the inductors provided by Foundry Companies, input impedance of the circuit is larger than 50 Ω impedance at resonant frequency. Therefore, to use inductor provided by Foundry Companies, we need to solve this problem.

The additional shunting capacitor C_F can solve the problem mentioned above. From the input impedance of Case B, which is complex, 50 Ω impedance can be obtained as follows. The input impedance of Fig. 2. is given below.

$$Z_{in2} = sL_g + \left[\frac{1}{sC_F} // \left(sL_s + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}}L_s\right)\right] \qquad (5)$$

The real term of (5) can be obtained as follows.

$$\left(\frac{L_s g_m}{C_{gs}} + sL_s + \frac{1}{sC_{gs}}\right) // \frac{1}{sC_F} = \frac{\frac{L_s}{C_F} + \frac{1}{s^2 C_{gs}C_F} + \frac{g_m L_s}{sC_{gs}C_F}}{\frac{L_s g_m}{C_{gs}} + sL_s + \frac{1}{s}\left(\frac{1}{C_F} + \frac{1}{C_{gs}}\right)}$$

where $(L_s g_m)/C_{gs}$ is equal to R, which is lager 50 Ω due to using inductor provided by Foundry Companies, assuming that

$$R^2 << \left(wL_s - \frac{1}{w}\left(\frac{1}{C_F} + \frac{1}{C_{gs}}\right)\right)^2 \quad \& \quad wL_s << \frac{1}{w}\left(\frac{1}{C_F} + \frac{1}{C_{gs}}\right)$$

The real term of input impedance is

$$\mathrm{Re}[\text{Input Impedance}] = \frac{R}{\left(1 + C_F / C_{gs}\right)^2} \qquad (6)$$

From (6), as shunting capacitor C_F value increases, real component of input impedance decreases. Therefore, this topology can get easily 50 Ω impedance with the inductor provided by Foundry Companies.

The imaginary term of (5) can be obtained as follows..

$$\left(\frac{L_s g_m}{C_{gs}} + sL_s + \frac{1}{sC_{gs}}\right) // \frac{1}{sC_F} = \frac{\frac{L_s}{C_F} + \frac{1}{s^2 C_{gs}C_F} + \frac{g_m L_s}{sC_{gs}C_F}}{\frac{L_s g_m}{C_{gs}} + sL_s + \frac{1}{s}\left(\frac{1}{C_F} + \frac{1}{C_{gs}}\right)}$$

Assuming that,

$$wZ_{in}^{\ 2} + w^3 L_s^{\ 2} << -\frac{2wL_s}{C_{gs}} + \frac{1}{wC_{gs}^{\ 2}} \quad \& \quad -wL_s << \frac{1}{wC_{gs}}$$

The imaginary term of input impedance is

$$\mathrm{Im}[\text{InputImpedance}] = -j\left[\frac{-2C_{gs}C_F wL_s}{\left(C_{gs} + C_F\right)^2} + \frac{1}{w\left(C_{gs} + C_F\right)}\right] \qquad (7)$$

Also, as shunting capacitor C_F value increases, imaginary

component of input impedance decreases then the value of input matching inductor (L_g) can be smaller for 50 Ω input impedance. It is possible to decrease noise figure of LNA, since small size inductor has small metal sheet resistance compared to large size inductor. Hence, because L_g value is smaller than without C_F, LNA of the Case B noise figure becomes low.

The G_m of Case B is given below.

$$G_{m2} = \frac{i_D}{v_{in}} = Q_{in2} \cdot g_m \qquad (8)$$

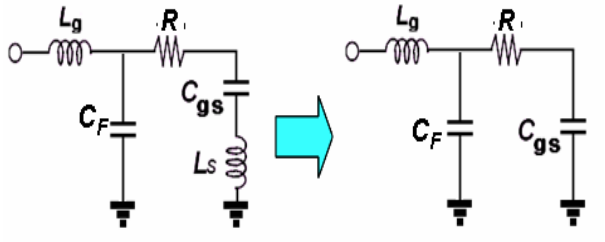

Figure 4. The input equivalent circuit of Case B

For obtaining G_{m2}, we need to see the circuit Fig. 4. in which L_s is ignored due to small impedance compared to impedance of C_{gs}. Here, $R= w_T L_s = g_m L_s / C_{gs}$, R is larger than 50 Ω input impedance, that is R_{in}. From Fig. 4, we can get Q_{in2} as below.

$$Q_{in2} = \frac{1}{wC_{gs}R_{in} \cdot \sqrt{R/R_{in}}} = \frac{Q_{in1}}{\sqrt{R/R_{in}}} \qquad (9)$$

From (9), gain of the Case B is smaller than the gain of the Case A.

III. Simulation Results

Based on 0.13 um CMOS technology, circuit simulation was carried out by using ADS simulator including the parasitic effects of the devices. The LNA S-parameter and noise simulation results are simulated at 5.2GHz, which is ISM frequency band.

Fig. 5 and Fig. 6 show schematics of the LNAs as mentioned in section II. To show the improvement by using C_F in Fig. 6, the output stage conditions, transistor sizes and bias conditions are set to be equal. The output matching elements L_D and C_O, dc blocking capacitor C_b and R_b for dc bias were used.

Table 1 shows simulation results, which are the input return loss (S_{11}), output return loss (S_{22}), reverse isolation (S_{12}), power gain and noise figure of Case A and Case B. From table 1, LNA power gain is superior for the Case A, but noise figure is superior for Case B as mentioned in section II. These simulation results are useful in that they can provide enough insights for designing CMOS RF LNA.

[dB] scale

	S_{11}	S_{22}	S_{12}	S_{21}	NF
Case A	-16.29	-27.64	-38.49	17.76	2.64
Case B	-15.34	-26.89	-38.44	17.18	2.31

Table 1. The LNAs Simulation Results

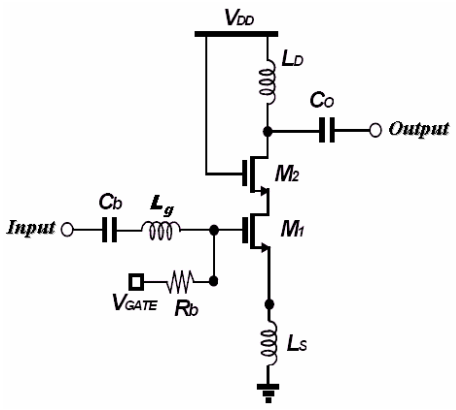

Figure 5. The LNA schematic of Case A

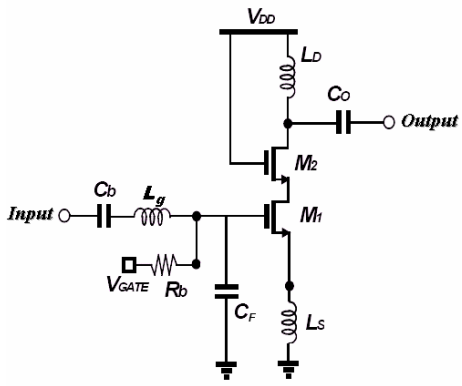

Figure 6. The LNA schematic of Case B

IV. Conclusion

In this paper, the analysis of input power matching for CMOS RF Low Noise Amplifier (LNA) design is introduced. With two input power matching techniques, the performance of

LNAs is estimated. These methods can provide enough insights for designing CMOS RF LNAs.

Acknowledgement

This work was supported partly by NSI_NCRC program of KOSEF, Korea, and ITRC.

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